

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TAKASHI NOGUCHI,
RAFAEL REIF, JULIE TSAI,
and ANDREW J. TANG

Appeal No. 2000-0769
Application 08/997,326¹

HEARD: February 12, 2002

Before KRASS, BARRETT, and SAADAT, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

¹ Application for patent filed December 23, 1997, entitled "High Performance Poly-SiGe Thin Film Transistor and a Method of Fabricating such a Thin Film Transistor," which is a continuation of Application 08/411,203, filed March 27, 1995, now U.S. Patent 5,828,084, issued October 27, 1998.

Appeal No. 2000-0769
Application 08/997,326

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 8 and 10-21.

We reverse.

BACKGROUND

The invention relates to a method of fabricating a thin film transistor (TFT) comprising the steps of: (1) depositing an active region comprising a polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ (poly- $\text{Si}_{1-x}\text{Ge}_x$) alloy material and then a channel layer of silicon, to form a composite; (2) treating the composite by crystallization or excimer laser annealing; and (3) depositing a gate.

Claim 8 is reproduced below.

8. A method of fabricating a one-gate thin film transistor, having an active region and a gate, wherein said active region comprises a poly- $\text{Si}_{1-x}\text{Ge}_x$ alloy material and channel layer of silicon, in which the channel layer of silicon is interposed between the poly- $\text{Si}_{1-x}\text{Ge}_x$ alloy material and the gate, comprising:

depositing a gate,

depositing an active region comprising a poly- $\text{Si}_{1-x}\text{Ge}_x$ alloy material layer and a channel layer of silicon, to form a composite, and

Appeal No. 2000-0769
Application 08/997,326

treating the composite with at least one method selected from the group consisting of crystallization and excimer laser annealing,

wherein said depositing a gate occurs subsequent to said depositing an active region and said treating the composite, wherein x ranges from 0.05 to 0.4 atomic %.

The Examiner relies on the following references:

1991	Solomon et al. (Solomon)	5,019,882	May 28,
1995	Burghartz et al. (Burghartz)	5,461,250	October 24,
			(filed August 10,
1992)			
	Ohtani et al. (Ohtani)	5,643,826	July 1, 1997
1994)			(filed October 25,

Tsu-Jae King and Krishna C. Saraswat, Polycrystalline Silicon-Germanium Thin-Film Transistors, IEEE Trans. on Electron Devices, Vol. 41, No. 9, September 1994, pp. 1581-1591 (hereinafter "King").

Claims 8 and 10-21 stand rejected under 35 U.S.C.

§ 103(a) as being unpatentable over King, Solomon, and Ohtani.

The Examiner cites Burghartz for additional background material (examiner's answer, p. 6).²

² References relied upon to support a rejection should be positively included in the statement of the rejection. See In re Hoch, 428 F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970); Ex parte Movva, 31 USPQ2d 1027, 1028 n.1 (Bd. Pat. App. & Int. 1993).

Appeal No. 2000-0769
Application 08/997,326

We refer to the final rejection (Paper No. 17) (pages referred to as "FR__") and the examiner's answer (Paper No. 19) for a statement of the Examiner's rejection, and to the brief (Paper No. 16) (pages referred to as "Br__"), the supplemental brief³ (Paper No. 18) (pages referred to as "SBr__"), and the reply brief (Paper No. 20) (pages referred to as "RBr__") for a statement of Appellants' arguments thereagainst.

OPINION

The claims stand or fall together as a group (Br4) and, thus, stand or fall together with independent claim 8.

It is noted that although claim 8 is directed a method of fabrication, the steps of fabrication are not listed in order. The step of "depositing a gate" is listed first, but it is later recited that "said depositing a gate occurs subsequent to said depositing an active region and said treating the composite." The limitation of "depositing an active region comprising a poly-Si_{1-x}Ge_x alloy material and a channel layer of

³ The Examiner reopened prosecution in response to the appeal brief to reformulate the rejection and made the action final (Paper No. 17). Appellants exercised their option under 37 CFR § 1.193(b)(2)(ii) (1999) to reinstate the appeal.

silicon" itself does not specifically define the order of depositing (e.g., depositing a layer of poly-SiGe and then a channel layer of silicon). However, the order can be determined from the preamble which states that the channel layer of silicon is interposed between the poly-SiGe alloy material and the gate.

King discloses a thin-film transistor (TFT) having an active channel region of poly-Si_{1-x}Ge_x alloy material and a gate. The poly-Si_{1-x}Ge_x alloy material may be produced by a high-temperature process in which the channel layer is deposited in polycrystalline form (p. 1581, right col.), which meets the claim limitation of "depositing an active region comprising a poly-Si_{1-x}Ge_x alloy material." The poly-Si_{1-x}Ge_x alloy material may be also produced by a low-temperature process in which the channel layer is deposited in amorphous form (p. 1581, right col.) and converted to polycrystalline form, which does not meet the limitation of "depositing an active region comprising a poly-Si_{1-x}Ge_x alloy material." As discussed in connection with Appellants' Table 1 (specification, p. 13), Si_{1-x}Ge_x films may deposited in either

polycrystalline or amorphous form; claim 8 requires deposition of the polycrystalline form.

The Examiner finds: (1) King does not teach forming a silicon layer on top of the poly-SiGe alloy material layer (FR5; EA4); and (2) King teaches recrystallization of the poly-SiGe alloy material layer in Table 1, step 3, but does not teach treating the composite by excimer laser annealing (FR6; EA6).

The Examiner finds that Solomon teaches an active region of a pseudomorphic SiGe alloy 2 and a channel layer of silicon 3, where the silicon layer provides high mobility charge carriers at the interface between the SiGe and the upper silicon layer to make an improved device (FR5; EA4-5). The Examiner concludes that one of ordinary skill in the art would have been motivated by Solomon to provide a channel layer of silicon above the poly-SiGe of King to increase the mobility of charge carriers in the channel, thereby improving the electrical characteristics of the device (FR6; EA5).

Appellants argue that pseudomorphic materials are single crystal materials and that a pseudomorphic lattice has a different structure and different operating characteristics

than a polycrystalline, or multicrystal lattice (SBr6). It is stated that pseudomorphic layers contain a lattice that is mismatched with respect to the substrate, forming a strained layer which effect changes the lattice constant, and, by contrast, a polycrystalline layer is not necessarily strained (Br5). Also, pseudomorphic and polycrystalline layers are typically formed by different methods (Br6). Appellants argue that the pseudomorphic SiGe layer of Solomon has a different structure and different operating characteristics than the claimed polycrystalline SiGe layer and, thus, it would not have been obvious to incorporate the teachings of Solomon into King (SBr6) because processes appropriate for a pseudomorphic SiGe layer are not necessarily appropriate for a polycrystalline SiGe layer (SBr7). More particularly, it is argued that one of ordinary skill in the art would not have looked to Solomon to improve the operation of the King device because King and Solomon are not readily combinable due to the different characteristics between polycrystalline SiGe and pseudomorphic SiGe (SBr6-7). That is, there is no motivation to combine the teachings of Solomon and King (SBr6; RBr3).

Appeal No. 2000-0769
Application 08/997,326

The Examiner responds that Solomon is used to teach a silicon layer on top of a SiGe alloy layer to increase the mobility of charge carriers at the interface between the SiGe the upper silicon layer to make an improved device and King teaches that it was conventional to use poly-SiGe as an active layer in TFT structures (EA7). The Examiner states that the rejection is not overcome by attacking the references individually (EA7).

We are not persuaded by the Examiner's response. The Examiner does not answer the argument that the teaching of application of a silicon channel layer to a pseudomorphic SiGe layer in Solomon does not suggest applying a silicon channel to a polycrystalline SiGe layer, such as King. Cases dealing with arguments attacking the references individually apply only after motivation has been shown for the combination and the issue is what is taught by the combination of the references.

The Examiner further states (EA7):

[I]t is noted that the specification appears to contain no disclosure of either the critical nature of the claimed layer being polycrystalline nor does it provide any unexpected results arising therefrom. In contrast, the specification (pg. 2) merely hypothesizes that "... a very-thin film silicon layer interposed between a poly

Appeal No. 2000-0769
Application 08/997,326

Si_{1-x}Ge_x alloy and a gate....might result in superior poly-Si_{1-x}Ge_x alloy TFT..." which is not novel as taught by Solomon and/or Burghartz.

As to the first sentence, that the specification does not disclose the critical nature of the polycrystalline layer or any unexpected results, we find that the specification clearly discusses why poly-SiGe is an improvement over poly-Si. The specification need not discuss pseudomorphic SiGe. The Examiner cannot disregard the poly-SiGe limitation.

The second sentence presents an interesting observation. As admitted by counsel at the oral hearing, the specification nowhere describes the purpose or advantage of applying a silicon layer to the poly-SiGe alloy layer of the prior art. Thus, Appellants are not in a good position to argue that the Examiner's reasons based on silicon over a pseudomorphic SiGe layer are wrong because Appellants cannot show that some other problem was being solved. It appears that any suggestion for adding a silicon channel layer to a poly-SiGe alloy layer would be sufficient motivation. Nevertheless, we are not persuaded that the Examiner's reasons, based on a silicon channel layer on a pseudomorphic SiGe layer, are persuasive of

the obviousness of providing a silicon channel layer on a poly-SiGe layer.

We accept Appellants' statement that pseudomorphic SiGe and polycrystalline SiGe are mutually exclusive crystal forms. Solomon discusses that a pseudomorphic alloy layer is under strain (col. 1, lines 43-52), implying a single crystal layer because a polycrystalline layer cannot be under strain because any strain ends at the grain boundaries. Solomon discusses that it is desirable to have a germanium alloy channel with a single crystal interface to silicon (col. 2, lines 14-19), which further supports the statement that a pseudomorphic layer is a single crystal. Solomon states that the transport properties of the channel are improved because the holes are confined to the interface between the pseudomorphic SiGe alloy layer and the silicon layer 3 and because the alloy layer is strained causing the energy of the light hole band to be lowered (col. 4, lines 33-40). It appears that the beneficial results of the silicon channel layer in Solomon are due solely to the pseudomorphic nature of the alloy layer. Thus, there is no reason why one of ordinary skill in the art would expect that applying a silicon channel layer to a poly-SiGe alloy

Appeal No. 2000-0769
Application 08/997,326

material would provide the same results. There must be both a suggestion for the modification and a reasonable expectation of success. See In re Vaeck, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). Here, because the advantageous results of silicon on a pseudomorphic SiGe layer are based on the properties of the pseudomorphic SiGe layer, we find no motivation in Solomon for applying silicon to a poly-SiGe layer or a reasonable expectation that doing so has a reasonable expectation of success. The Burghartz patent, although not technically part of the rejection, refers to the Solomon patent and appears to disclose no more than Solomon. Thus, Burghartz does not cure the deficiencies of the combination. Ohtani is relied on only for a teaching of excimer laser annealing and does not cure the deficiencies of the combination of Solomon and King. We conclude that the Examiner has failed to establish the motivation to add a silicon channel layer to a poly-SiGe ally layer in King and, thus, has failed to establish a prima facie case of obviousness. The rejection of claims 8 and 10-21 is reversed.

Citation of relevant reference

Appeal No. 2000-0769
Application 08/997,326

We cite Banerjee et al. (Banerjee), U.S. Patent 5,665,981, issued September 9, 1997, and having an effective filing date of October 24, 1994 (copy attached) as relevant to the patentability of claim 8. Banerjee teaches a thin film transistor (TFT) 20 having an active channel region 26 comprising a middle layer 32 of poly-SiGe between layers 28, 30 of poly-Si, where the channel region overlies gate 16 (col. 3, line 35 to col. 4, line 4). This bottom gate configuration is similar to the embodiment of Appellants' Fig. 3 and, in our opinion, it would have been obvious to apply the bottom gate TFT teachings of Banerjee to a top gate TFT as shown in King to provide the same advantages. Banerjee discloses that the poly-SiGe alloy layer 32 has a lower energy bandgap than the poly-Si and the band-edge discontinuity for poly-SiGe is primarily in the valence band which is ideal for confining the holes within layer 32 in the middle, away from the high defect poly-oxide interfaces, which results in lower leakage current and sharper sub-threshold slopes (col. 4, lines 4-13). Thus, Banerjee expressly teaches the silicon channel layer on a poly-SiGe layer between the poly-SiGe layer and the gate, and the advantages thereof. Banerjee further

Appeal No. 2000-0769
Application 08/997,326

discloses that large grain size is preferred for conductivity reasons (col. 1, line 66 to col. 2, line 51). Banerjee discloses heating the poly-SiGe alloy to an effective temperature for an effective period of time to increase grain growth (col. 4, line 63 to col. 4, line 12), which we interpret to mean a step of crystallization.

Appeal No. 2000-0769
Application 08/997,326

CONCLUSION

The rejections of claims 8 and 10-21 are reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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Appeal No. 2000-0769
Application 08/997,326

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