

The opinion in support of the decision being entered today was not written for publication and is **not** binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WOLFGANG ECKER

Appeal No. 2000-1361
Application No. 08/933,880¹

HEARD: March 20, 2002

Before BARRETT, DIXON, and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1 through 8, which are all of the pending claims in this application.

We affirm-in-part.

¹ Application for patent filed September 19, 1997, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of German Application 19639935.1, filed September 27, 1996.

BACKGROUND

Appellant's invention is directed to a synchronous circuit with increased processing speed, which includes a combinatorial block located between two registers. An analysis unit receives and analyzes the value of the output of the input register to determine when to send an enable signal to the output register (specification, page 2). The analysis unit sends the enable signal to the output register at the time the analysis unit determines that an output value of the combinatorial blocks is present, allowing the outcome to be taken earlier (specification, page 4). Thus, based on the value combinations present at the output of the input register, the outcome is clocked into the output register sooner and the transit time required for processing an operation through the combinatorial block is decreased (abstract and specification, page 4).

Representative independent claim 1 is reproduced as follows:

1. A circuit arrangement with at least one combinatorial block arranged between registers, comprising:

an input register of said registers having an output connected to an input of the combinatorial block, and an output register of said registers having an input connected to an output of the combinatorial block; and

an analysis unit, the output of the input register also connected to the analysis unit that analyzes a value of the output of the input register and that sends an enable signal

to the output register when an output value of the combinatorial block is present according to the value of the output of the input register.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Kontani et al. (Kontani)	5,195,049	Mar. 16, 1993
Richardson	5,262,973	Nov. 16, 1993

Claims 1, 4 and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Richardson.

Claims 2, 3, 5, 7 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Richardson in view of Kontani.

Claims 3 and 6 through 8 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Rather than reiterate the conflicting viewpoints advanced by the Examiner and Appellant regarding the above-noted rejections, we make reference to the answer (Paper No. 13, mailed September 1, 1999) for the Examiner's complete reasoning and to the appeal brief (Paper No. 12, filed August 18, 1999) for Appellant's arguments thereagainst.

OPINION

The rejection of claims 3 and 6 through 8 under the second paragraph of 35 U.S.C. § 112 as being indefinite has not been

argued. Accordingly, the § 112 rejection of claims 3 and 6 through 8 is sustained pro forma. Appellant indicates (both in the brief and during the oral hearing) that upon reversal of the rejections under §§ 102 and 103, Appellant will submit appropriate amendments to overcome the § 112 rejection.

At the outset, we note that Appellant does not separately argue the patentability of the independent claims and indicates that claims 1 through 8 stand or fall together (brief, page 4). Therefore, we will consider the claims as one group and will treat claim 1 as the representative claim of the group.

Appellant argues that Richardson cannot anticipate the claimed invention since instead of an enable signal, output values are sent from comparator blocks 510-560 to output registers 570-630 (brief, page 6). Appellant further compares Richardson with the claimed analysis unit, which does not supply the output values and merely provides an enable signal for the output register as soon as the combinatorial block has finished the processing of the input values (brief, pages 6 & 7).

In response to Appellant's arguments, the Examiner indicates that an enable signal is sent by each of comparator blocks 510-560 to the corresponding one of output registers 570-630 which causes the register to output its stored value. The Examiner

further characterizes Richardson's claims 1 and 14 limitations of "an enabling signal" that is provided by the comparators to corresponding output registers, as the claimed enable signal sent to the output register (answer, page 3).

With respect to the rejection of claims over Richardson, the Examiner makes the following correspondence between the claim elements and the circuit of figure 5 in Richardson: the "input register" reads on registers 640 and 650; the "combinatorial block" reads on multiplier 500 and comparator blocks 510-560; the "output register" reads on registers 570-630 and 670; the "analysis unit" reads on comparator blocks 510-560; and the "enable signal" reads on the output from comparator blocks 510-560 to the registers 570-630 (answer, page 3).

We must make a couple of modifications and simplifications of these findings to try to correspond claim 1 more precisely to Richardson. For example, the Examiner uses the comparator blocks 510-560 as part of both the "combinatorial block" and the "analysis unit." They cannot be part of both elements. To simplify the analysis, we read the "analysis unit" on the comparator blocks 510-560. The "input register" clearly reads on registers 640 and 650. We agree that the "output register" must read on registers 570-630, if anything, because they are the only

elements that receive a signal from the "analysis unit" (comparator blocks). Since registers 570-630 output results, it seems fair to call them output registers. We agree that the "combinatorial block" reads at least on multiplier 500.

Before addressing the Examiner's rejection based upon prior art, it is essential that we understand the claimed subject matter as well as the teachings of the prior art. As required by our reviewing court, we will initially direct our attention to Appellant's claim 1 in order to determine its scope. "[T]he name of the game is the claim." In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). Claims will be given their broadest reasonable interpretation consistent with the specification, and limitations appearing in the specification are not to be read into the claims. In re Etter, 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985).

Appellant's claim 1 requires that an analysis unit be connected to the output of the input register and "analyze a value of the output of the input register" and "send an enable signal to the output register." The claim further requires that the enable signal be sent as soon as the analysis unit, based on the "value of the output of the input register," has determined that "an output value of the combinatorial block is present" at

that time. We are also in agreement with Appellant's characterization that the claimed analysis unit provides merely an enable signal to the output register whereas the output values are provided by the combinatorial block (oral hearing and brief, page 7). The claimed analysis unit analyzes values at the output of the input register to determine the time at which an output value is present for enabling the output register to receive the outcome values as soon as they are provided by the combinatorial block. Thus, the resulting output value of the combinatorial block can be taken earlier at the output register based on the values at the output of the input register, rather than waiting for a predetermined delay as set by a number of clock pulses (specification, page 4).

A rejection for anticipation under section 102 requires that the four corners of a single, prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. See Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994). An anticipating reference must describe the claimed matter with sufficient clarity and detail to

establish that the subject matter existed and that its existence was recognized by persons of ordinary skill in the field of the invention. See In re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990); Diversitech Corp. v. Century Steps, Inc., 850 F.2d 1566, 1567, 7 USPQ2d 1315, 1317 (Fed. Cir. 1988).

After reviewing the teachings of Richardson and considering the arguments of record, we disagree with the Examiner that enable signal sent from comparators 510-560 to output registers 570-630 and 670 (depicted in Fig. 5) is the same as the claimed enable signal. Richardson, in col. 4, lines 2-11 teaches:

Registers 570, 580, 590, 600, 620 and 630 store the concurrently determined results for the instances of trivial operands. If any of the tests performed by comparators 510-560 result in a positive response indicating that one of the operands is a trivial operand, a halt signal is issued by the comparator to the multiplier 500 and an output signal is issued to the corresponding register 570, 580, 590, 600, 620 and 630 which outputs immediately the result. [Emphasis added.]

Therefore, when one of the tests, say $x=1$, indicates a trivial operand, the "analysis unit" (comparator block 520) outputs a signal to the "output register" (register 580) which outputs immediately the result. The result has been previously stored in register 580 and is sent to output register 670 without going through multiplier 500. Although comparators 510-560, similar to the claimed analysis unit, analyze the values provided by input

registers 640 and 650, we find that these comparators indeed stop multiplier 500 from generating any output value concurrent with the enable signal sent to the output registers. In other words, multiplier 500 is bypassed by sending a halt signal to the multiplier in the event that a trivial operand is received from input registers 640 and 650 at comparators 510-560. At the same time, an enable signal is sent to the corresponding one of output registers 570-630 causing them to send their previously stored values to register 670.

Based on the analysis above, we find that Richardson's enable signal is provided to the output registers if either operand is trivial. Richardson has nothing to do with the time at which an output value of the multiplier is present or determining that time according to the value of the output of the input registers. The output registers of Richardson provide to register 670 the results that have been previously stored if the comparators determine a trivial operand and send an enable signal to the output registers. At the same time, a halt signal prevents the operation of the multiplier. This condition is different from the requirements of claim 1, in which the enable signal is sent to the output register as soon as it is determined

according to the value of the output of the input registers that an output value of the combinatorial block is present.

Assuming arguendo, that one of the lines from registers 640 and 650 to blocks 580, 590, 620, and 621 is included in the "combinatorial block" for presenting a trivial output to the output register, Richardson would still not teach the claimed conditions for the enable signal. For simplicity, we can read the "combinatorial block" on multiplier 500 as well as the line from input register 650 to register 580. We note that the specification does not disclose the internal construction of the combinatorial block and does not exclude lines in the combinatorial block which directly present the input value to the output as in Richardson. When the "analysis unit" (comparator block 520) determines that x equals 1, indicative of a trivial operand, the "analysis unit" outputs a signal to the "output register" (register 580) which immediately outputs the result that has been previously provided by the line in the combinatorial block and stored in register 580. Therefore, the result is sent to the output register if an output value of the combinatorial block is present according to the value of the output of the input register. An output value of the combinatorial block is present on the line leading to block 580

and the "analysis unit" (comparator block 520) sends an enable signal to the "output register" (register 580) based on the value of the output of the "input register" (registers 640 and 650). We still see no disclosure in Richardson related to using the value of the output of the input register to determine the time at which an output value of the combinatorial block is present for sending an enable signal to the output register.

Therefore, we find that the reference fails to teach all the claimed requirements for sending an enable signal from the analysis unit to the output register at a specific time and cannot anticipate the claimed subject matter. Accordingly, since the Examiner has failed to meet the burden of providing a prima facie case of anticipation, the rejection of claims 1, 4 and 6 under 35 U.S.C. § 102 over Richardson cannot be sustained.

Regarding the rejection of claims 2, 3, 5, 7 and 8 under 35 U.S.C. § 103 over Richardson and Kontani, we note that Kontani merely teaches detection of anomalous signals by using a digital filter. However, the reference fails to provide any teachings or suggestions for modifying Richardson to overcome the deficiencies discussed above. Therefore, we do not sustain the rejection of claims 2, 3, 5, 7 and 8 under 35 U.S.C. § 103 over Richardson and Kontani.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1 through 8 under 35 U.S.C. §§ 102 and 103 is reversed. The decision of the Examiner rejecting claims 3 and 6 through 8 under 35 U.S.C. § 112 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

LEE E. BARRETT)	
Administrative Patent Judge)	
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)	
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)	BOARD OF PATENT
JOSEPH L. DIXON)	APPEALS
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)	INTERFERENCES
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APPEAL NO. 00-1361 - JUDGE SAADAT
APPLICATION NO. 08/933,880

APJ SAADAT

APJ BARRETT

APJ DIXON

DECISION: **REVERSED**

PREPARED: Jun 3, 2003

TYPED: 03/26/2002

ART UNIT 2700

OB/HD

THREE MEMBERS CONFERENCE

YES/NO

PALM

ACTS 2

DISK (FOIA)

REPORT