

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT S. CHAU, EBRAHIM ANDIDEH, MITCH C. TAYLOR,
CHIA-HONG JAN, and JULIE TSAI

Appeal No. 2001-2037
Application No. 08/884,912

ON BRIEF

Before THOMAS, KRASS, and BLANKENSHIP, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 8-10, 12, 13, 15, 16, 18-22 and 24. Claims 1-6 stand withdrawn as being directed to a nonelected invention and have been cancelled. Claims 7 and 17 have been cancelled. Claims 23 and 26-31 have been allowed.

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The invention is directed to a method for reducing silicide encroachment in a semiconductor device.

Representative independent claim 8 is reproduced as follows:

8. The method of forming an MOS transistor comprising the steps of:

forming a gate electrode on a gate dielectric layer formed on a first surface of a substrate;

forming an isolation region having a top surface extending less than 1500Å above said first substrate surface;

forming a pair of recesses on opposite sides of said gate electrode, said recesses extending beneath said first surface, and

forming a silicide layer in said pair of recesses wherein said silicide layer has a top surface with a height less than the top surface of said isolation region.

The examiner relies on the following references:

Young et al. (Young)	4,851,257	Jul. 25, 1989
Subbanna	5,338,698	Aug. 16, 1994
Song	5,686,331	Nov. 11, 1997
		(filed Dec. 24, 1996)
Venkatesan et al. (Venkatesan)	5,736,435	Apr. 7, 1998
		(filed Jul. 3, 1995)

Claims 8, 9 and 24 stand rejected under 35 U.S.C. 102(b) as anticipated by Subbanna.

Claims 10, 12, 13, 15, 16 and 18-22 stand rejected under

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35 U.S.C. 103. As evidence of obviousness, the examiner cites Young and Song with regard to claims 10, 12, 13, 15 and 18-22, adding Ventkatesan with regard to claim 16.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

Turning first to the rejection under 35 U.S.C. 102(b), the examiner relies on Figures 3 and 9 of Subbanna. Subbanna teaches the formation of a MOS transistor wherein a gate electrode (N+) is formed on a gate dielectric layer (see the oxide layer under the gate) formed on a first surface of a substrate 31. An isolation region is formed (see oxide layers on either side of Subbanna's Figure 9) and the top surface of the isolation region extends less than 1500 Angstroms (because 0 is clearly less than 1500 Angstroms) above the first surface of the substrate. As shown in Figure 9 of Subbanna, there are a pair of recesses formed on opposite sides of the gate electrode, wherein the recesses extend the first substrate surface, as claimed. Moreover, a silicide layer WSi is formed in the pair of recesses

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and the top surface of the silicide layer has a height less than the top surface of the isolation region, as claimed.

Accordingly, we agree with the examiner that the subject matter of claims 8, 9 and 24 is anticipated by Subbanna.

Appellants argue that Subbanna discloses a silicide layer which is coplanar with the top surface of the isolation regions rather than being of less height than the top surface of the isolation region. However, appellants must be looking at silicide layer W, rather than WSi. Layer WSi, formed on the bottom of the recesses, may also be considered a "silicide layer" and this particular silicide layer meets the claim language.

It matters not that Subbanna does not mention the height of the silicide layer as compared with the height of the substrate surface. Sometimes the story is told by reference to the drawings. While drawings are not always an accurate assessment of relative measurements because they may not be drawn to scale, in this particular case, it is very clear that silicide layer WSi in Figure 9 has a height less than the height of the substrate surface since layer W occupies space between the top of layer WSi and the top surface of the substrate.

Even if the problem with which appellants are concerned is

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not the same problem with which a reference is concerned, a claim may still be anticipated under 35 U.S.C. 102(b) if each and

every element of the claim and its attendant function is taught by the reference, as here.

Turning to the rejections under 35 U.S.C. 103, the examiner relies on the combination of Young and Song to reject independent claim 10 and its dependent claims, adding Ventkatesan to the combination with regard to claim 16.

In particular, the examiner contends that Young discloses the formation of gate dielectric layer 211, formation of a silicon layer 212 over the gate dielectric layer, formation of spacers in Figure 4b, doping the silicon layer with N-type or P-type dopants, and the formation of a silicide in Figure 4d. Pages 4-5 of the answer describes other teachings of Young. The examiner indicates that Young teaches the claimed subject matter but for specifically showing the spacers having a height which is greater than the sum of the gate electrode and the silicide layer. However, the examiner contends that Song discloses such a relationship, i.e., spacers having a height which is greater than the sum of the gate electrode and the silicide layer and that it would have been obvious to modify Young with this teaching of

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Song because "it would prevent a bridging phenomenon between a gate electrode and drain/source areas as taught [by] Song (col. 3, lines 40-45)" [answer-page 5].

Appellants argue that there would have been no motivation for combining Young and Song because neither reference is concerned with a problem of silicide overflow and the potential bridging problems resulting therefrom, as are appellants.

Appellants' argument in this regard is not convincing because independent claim 10 recites nothing about overflow problems.

In fact, we find Young's teaching to be merely cumulative to that of Song because, in our view, as broadly set forth in claim 10, the claimed subject matter is met by Song's disclosure alone. Viewing Figure 2I of Song, a semiconductor device is formed wherein a gate dielectric 10 is formed on a silicon substrate 1. Then, a silicon layer having a first thickness is formed over the gate dielectric layer 10 and a sacrificial, or disposable, layer 12 is formed over the silicon layer. The silicon layer and disposable layer are patterned into an electrode (column 2, lines 52-56) and a pair of spacers 13, having a first height, are formed on opposite sides of the electrode. The disposable layer

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12 is removed from over the silicon layer (column 3, lines 5-6) and the silicon layer is doped. A silicide of second thickness is formed on the doped silicon layer (19) and on the substrate adjacent to the outside edges of the spacers (18). It is clear from Figure 2I of Song that the first height (of the spacers 13) is greater than the sum of the first thickness (of the silicon layer) and the second thickness (of 18, 19).

While Song, alone, meets the limitations of independent claim 10, we will sustain the rejection of claims 10, 12, 13, 15 and 18-22 under 35 U.S.C. 103 since anticipation is the epitome of obviousness. In re Fracalossi, 681 F.2d 792, 215 USPQ 569 (CCPA 1982). Lack of novelty is the ultimate of obviousness. In re Pearson, 494 F.2d 1399, 181 USPQ 641 (1974).

Turning to the rejection of claim 16, this claim adds the limitation of polishing the silicon layer prior to forming the sacrificial layer. The examiner cites Venkatesan for a chemical/mechanical polishing process to form a gate electrode 36 and contends that it would have been obvious to modify Young's process by including a polishing step because "it would selectively removed [sic, remove] a part of the silicon layer for forming a planar surface and would avoid misaligning" [answer-page 6].

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Appellants' response is to merely repeat the argument made with regard to independent claim 10 without addressing the specific limitation recited in claim 16. Accordingly, we will sustain the rejection of claim 16 under 35 U.S.C. 103 as the examiner appears to have set forth a reasonable case for obviousness and appellants do not respond in a substantive manner. Arguments not made are waived. In re Kroekel, 803 F.2d 705, 231 USPQ 640 (Fed. Cir. 1986).

The examiner's decision rejecting claims 8, 9 and 24 under 35 U.S.C. 102(b) and claims 10, 12, 13, 15, 16 and 18-22 under 35 U.S.C. 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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ERROL A. KRASS)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES

