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Appeal No. 93-1621

PAT.&T.M. OFFICE  
BOARD OF PATENT APPEALS  
AND INTERFERENCES

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ON BRIEF

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

Ex parte Masami Yamaoka  
and Shoji Toyoshima

Application for Patent filed September 14, 1989, Serial No. 07/407,157, which is a Continuation of Serial No. 07/148,085, filed January 25, 1988, now abandoned, which is a Continuation of Serial No. 06/859,215, filed May 2, 1986, now abandoned, which is a Continuation of Serial No. 06/452,404, filed December 22, 1982, now abandoned. Semiconductor Device Including Overvoltage Protection Diode.

Chris Comuntzis, for appellants.<sup>1</sup>

Primary Examiner - William D. Larkins.

Before Craig, Lynch and Hairston, Administrative Patent Judges.  
Lynch, Administrative Patent Judge.

This is an appeal under 35 U.S.C. §134 from the final rejection of claims 31-68, all the claims remaining in the application. Claims 1-30 have been cancelled. There are no other claims in the application.

<sup>1</sup>Hereafter appellant.

The claimed subject matter relates to a semiconductor device having an overvoltage protection function as illustrated by independent claim 31.

Claim 31 reads as follows:

31. A semiconductor device having an overvoltage protection function comprising:

a substrate having N-type conductivity with impurity concentration of approximately  $1.0 \times 10^{14}$  to  $2.0 \times 10^{14}$  atoms/cm<sup>3</sup>;

a cathode conductive layer formed on a first major surface of said substrate;

a P-type diffusion region formed in the substrate and occupying a first predetermined diffusion depth from a second major surface of said substrate;

an N-type diffusion region formed in the substrate, spaced apart from said P-type diffusion region, and occupying a second predetermined diffusion depth from said second major surface, said N-type diffusion region having an impurity concentration higher than the impurity concentration of said substrate;

an anode conductivity layer overlapping at least a portion of said P-type diffusion region for receiving a reverse-bias voltage, said reverse-bias voltage being set not less than 200 v and applied across said cathode conductive layer with respect to said anode conductive layer ( $V_{AC}$ );

an insulating layer overlapping at least a portion of the second major surface of said substrate between the P-type diffusion region and the N-type diffusion region; and

a gate electrode conductive layer overlapping at least a portion of said insulating layer which includes at least said portion of the second major surface of said substrate between the P-type diffusion region and the N-type diffusion region, said gate electrode conductive layer for inputting a constant potential difference set in the range of -200 to 200 v and



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declaration is that of patent engineer Takashi Iwasawa, submitted under 37 CFR 1.132 in parent application S/N 148,085 on November 16, 1988.

Claims 31-68 stand rejected under 35 U.S.C. §112, second paragraph, as being vague and indefinite. The examiner maintains that these claims fail to particularly point out and distinctly claim what appellant regards as his invention.

Claims 31-68 stand further rejected as being unpatentable under 35 U.S.C. §112, first paragraph, under the written description requirement of this section of the statute. With respect to the independent claims 31, 45, 55 and 63, the examiner maintains that there is no basis in the original disclosure for recitations such as that of claim 31 to the effect of "inputting a constant potential difference set in the range of -200 V to 200 V and applied across the gate conductive layer with respect to said anode conductive layer ( $V_{GA}$ )---." Further with respect to dependent claim 35, the examiner maintains that there is no basis in the original disclosure for the recitation of a surface concentration of  $1 \times 10^{17}$  atoms/cm<sup>3</sup>.

Claims 31-68 stand still further rejected as being unpatentable under 35 U.S.C. §112, first paragraph, under the enablement provision of this section of the statute. The

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examiner maintains that the application lacks a sufficient disclosure such as to enable one of ordinary skill in the art to make and use same.

Rather than reiterate the arguments of appellant and the examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

The rejection of claims 31-68 under the second paragraph of 35 U.S.C. §112, is reversed. We have carefully considered the complete record and find ourselves in agreement with the appellant.

In accordance with In re Moore, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971), where multiple rejections are at issue, it is appropriate to first consider the rejection of the claims under the second paragraph of §112. Also under Moore, claims are definite when they set out and circumscribe a particular area of technology with a reasonable degree of precision and particularity. Moreover, claims are never considered in a vacuum, but always in light of appellant's disclosure and the prior art as they would be construed by one of ordinary skill in the art. Accordingly, in light of In re Moore, supra, we now address the examiner's objections.

Although he has intertwined and confused the rejection under the second paragraph of §112 with the rejections under the

first paragraph of §112, we will attempt to discern the specific objections that the examiner has made to the claim limitations. Thus, with respect to independent claims 31, 45, 55, and 63, the examiner apparently objects to the recitations in each of these claims which he has paraphrased as essentially reading, "applying a constant potential difference between -200V and +200V between the gate and the anode, the reverse bias voltage between the cathode and the anode being greater than the constant potential difference between the gate and the anode." The examiner maintains that it is not possible to tell what is being applied to what in this disclosure, and therefore, such recitations do not make sense. We do not agree.

For example, the specification (page 5, lines 13-15) indicates that Figure 2 is a schematic representation of the semiconductor device of Figure 1. Figure 2 discloses a variable power source applied between the gate electrode 14 and the anode conductive layer 15. The specification states (page 5, lines 16-17) that the variable gate voltage  $V_G$  is set (apparently as an initial condition) at 0 volts. Later the specification (page 10, lines 7-11), indicates that the gate voltage can be varied to different values as shown in Figure 4 from -200v to +200v.

The specification (page 5, lines 15-18) further states that the protection diode of Figure 2 has a reverse bias applied

to the anode and that the reverse bias can be increased from an initial value. The specification (page 10, lines 7-11) continues with the explanation of Figure 4 which discloses the diode reverse breakdown voltage with variation of the reverse bias voltage and the gate voltage. Thus, Figure 4 discloses that when the reverse bias is varied between 200v and 600v as the gate voltage is varied from a value between -200v to +200v, various breakdown voltages are achieved (Spec., page 10, line 11 et seq.). Consequently, when the above-quoted claim limitation is construed in light of the disclosure by one of ordinary skill in the art, the limitation clearly makes sense. Thus, whether the examiner agrees from an operational standpoint is not relevant to this second paragraph rejection. Accordingly, the examiner's objection to the language of independent claims 31, 45, 55 and 63 under the second paragraph of §112 is unwarranted.

With respect to the dependent claims, the examiner further objects to any claim which recites a direct gate to anode connection because such a recitation allegedly contradicts the claims from which they depend. Apparently, because the independent claims recite that the gate voltage can vary between -200v to +200v, the examiner is maintaining that a gate to anode voltage difference of zero volts (i.e., such as would be equivalent to a direct connection) cannot be made. We do not agree.

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In the first place, we have carefully reviewed each of the dependent claims at issue, and find that none of the claims specifically recite a "direct" gate to anode connection. However, dependent claims 32, 46, 56 and 64 do recite that the "gate electrode conductive layer and the anode [or second] conductive layer are connected ( $V_{GA}=0$ )," but such a recitation does not require a direct connection. To the contrary, such a recitation when construed in light of the disclosure does not conflict with the recitations of the independent claims which recite that the gate and anode are connected via a power supply which can vary in value between -200v and +200v since this clearly includes the situation where one of those values is 0 volts. Therefore, this objection is without merit.

With further regard to the direct gate to anode connection, the examiner also objects to the recitations of dependent claims 41-54 and 59-68 which are specific to a gated protection diode in combination with other transistor circuitry. The examiner maintains that the only description of such a protection diode in combination with a transistor is where there is only a direct connection and not a variable voltage connection between the gate and the anode. We find that the examiner has taken an unduly restrictive interpretation of appellant's Figures 5A, 5B, 6-8, 9A and 9B, since the diode structure of Figures 1-4

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is clearly intended to be used in combination with the transistor circuits of Figures 5A, 5B, 6-8, 9A and 9B. See the specification, page 3, line 27 through page 4, line 14.

In view of the above, it is clear that in all of these objections the examiner has construed the claim limitations in a vacuum rather than considering them in light of the disclosure as required under In re Moore, supra. The examiner's hypertechnical objections in this regard serve no useful purpose in the furtherance of the prosecution of this application which is now in its fourth continuation. Therefore, none of the examiner's objections to the recitations of claims 31-68 under the second paragraph of §112 are viable, and accordingly, the rejection cannot be sustained.

We turn now to the rejection of all of the claims under the written description requirement of the first paragraph of §112. Except for claim 35, we hold this rejection cannot be sustained either. We have again carefully considered the complete disclosure and apart from claim 35 find ourselves in agreement with the appellant.

We consider first the examiner's objection to dependent claim 35 as reciting new matter. Claim 35 recites that the P type diffusion region 11 has a surface concentration of  $1 \times 10^{17}$  atoms/cm<sup>3</sup> whereas appellant's specification (page 7, lines 13-15)

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states that the surface concentration is  $1 \times 10^{13}$  atoms/cm.<sup>3</sup> Appellant argues that this difference is merely a typographical error made in the translation from the Japanese priority document, and in any case, the artisan would have known that the surface concentration of this region would have to be at least an order of magnitude or higher than the concentration level of the substrate which is  $1.5 \times 10^{15}$  atoms/cm.<sup>3</sup> Even though the examiner agrees that the artisan would have known that the concentration must be higher than that stated in the specification, he adamantly refuses to allow the appellant to explain away this inconsistency or to amend the disclosure to correct the error, and stoutly insists that the recitation of claim 35 is new matter.

As pointed out in the joint declaration of coinventors Yamaoka and Toyoshima and the declaration of the Japanese patent engineer, Iwasawa, the original Japanese document clearly lists the surface concentration of the P-type region as  $1 \times 10^{18}$  atoms/cm<sup>3</sup>, and thus, it was only an inadvertent typographical error in the translation which caused this error. The examiner does not comment on these declarations. In any case, our independent review of the Japanese priority document confirms the declarants' assertions that a concentration of  $1 \times 10^{18}$  atoms/cm<sup>3</sup> is the correct doping level, and that therefore, this is the level

clearly intended throughout the prosecution of this application. Certainly, if this typographical error involved the misspelling of some word, or an incorrect punctuation mark, the examiner would have been insistent that the correction be made. Consequently, we fail to understand the examiner's adamant refusal to allow this simple typographical correction to be made in this instance. However, we note that claim 35 recites the doping level for region 11 as  $1 \times 10^{17}$  atoms/cm<sup>3</sup> whereas the specification, when corrected, indicates that the doping level is  $1 \times 10^{18}$  atoms/cm<sup>3</sup>. Since there is no basis in the original disclosure for a doping level of  $1 \times 10^{17}$  atoms/cm<sup>3</sup>, the rejection is correct and is sustained.

Turning now to independent claims 31, 45, 55 and 63, as noted above, the examiner maintains that there is no basis in the original disclosure for recitations such as that of claim 31 which recites "inputting a constant potential difference set in the range of -200 V to 200 V and applied across the gate conductive layer with respect to said anode conductive layer ( $V_{GA}$ ), the reverse-bias voltage ( $V_{AC}$ ) applied across the cathode conductive layer and the anode conductive layer being set greater than the constant potential difference set across the gate electrode conductive layer and the anode conductive layer ( $V_{GA}$ )."

We do not agree with the examiner that this limitation is not

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described in the original disclosure. In the first place, the original disclosure of the great grandparent application (S/N 452,404, filed December 22, 1982) is identical to the disclosure of the present application and each of the intermediate applications is also identical. Moreover, as pointed out in our treatment of the rejection of all claims under the second paragraph of §112, supra, appellant's Figure 2 clearly discloses a variable power supply between the gate and the anode, and as shown by Figure 4, that power supply can be set to a number of different constant values between -200v and +200v with the anode to cathode voltage being not less than +200v and always greater than the gate to anode voltage. Therefore, there is clear support for this limitation in the original disclosure, and thus, the rejection cannot be sustained.<sup>3</sup>

The rejection of claims 31-68 under the enablement provision of the first paragraph of 35 U.S.C. §112, is also reversed. We have carefully considered the complete record and find ourselves in agreement with the appellant.

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<sup>3</sup>In view of this holding, we also see no reason why the proposed drawing amendments to Figure 4, filed February 25, 1991, have been refused entry by the examiner. The examiner's hypertechnical interpretation of appellant's original disclosure is simply not warranted.

What the examiner is really challenging in this rejection is not whether the disclosure is enabling, but whether appellant's description or theory of how the device operates in the specification is correct. Thus, the examiner's objection to the disclosure is based on his contention that the inversion layer 17 of Figure 1 is not formed as asserted by the appellant, and that this is shown to be clearly the case by the references to Grove and MacIver. In this regard, the examiner acknowledges that the claims at issue no longer specifically recite such an inversion layer, but he is apparently maintaining that the limitations at issue must depend on such an inversion layer for the device to operate in the manner claimed.

As we view the situation, however, the issue of this rejection is simply whether appellant's device operates as disclosed to provide the recited controlled breakdown voltage. From our perspective, appellant discloses a device in which the gate voltage modulates the depletion layer formed when the diode is back biased such that a variable breakdown voltage is obtained. We see no reason why the device does not operate in the manner depicted by Figure 4 which is substantiated by the Yamaoka declaration. As far as the claimed subject matter is concerned, it is immaterial that appellant's specification attempts to explain the theory of operation in terms of an inversion layer. Perhaps this is simply the result of some

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mistranslation from the original Japanese. Accordingly, we find that the examiner has not raised a reasonable challenge as to the enablement of the claimed device. Therefore, the rejection cannot be sustained. See, In re Buchner, 929 F.2d 660, 18 USPQ2d 1331 (Fed. Cir. 1991); and In re Scarbrough, 500 F.2d 560, 182 USPQ 298 (CCPA 1974).

Pursuant to 37 CFR 1.196(b), we enter the following new rejection. Claims 31, 32, 34-51 and 53-68 are rejected under 35 U.S.C. §103 as being obvious over the reference to Yoshida cited above. The reference to Yoshida discloses a conventional protection diode wherein the anode and the gate electrode are directly connected such that the voltage between the gate and anode is zero. Since none of these claims distinguish over such a connection, however, their rejection as being obvious variations over Yoshida is clearly proper. Certainly, the physical characteristics of the protection diode would have been obvious variations of the device disclosed by Yoshida. Similarly, the recitations of the protection diode in combination with other transistorized circuitry such as recited by claims 42-50, 53, 54 and 59-68 would also have been conventional. Finally, the recitation of such a device in combination with an ignition control circuit as recited by claims

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51 and 66 would also have been conventional. Accordingly, the rejection of claims 31, 32, 34-51 and 53-68 is correct.

We have carefully reviewed all the evidence in this application and have considered all the arguments advanced by appellant and the examiner, including those not directly addressed. We have sustained the rejection of claim 35 under the written description requirement of the first paragraph of §112. However, we have reversed all of the other rejections under the first and second paragraphs of §112. Accordingly, the decision of the examiner is affirmed-in-part. Moreover, pursuant to 37 CFR 1.196(b), we have entered a new prior art rejection of claims 31, 32, 34-51 and 53-68.

Any request for reconsideration or modification of this decision by the Board of Patent Appeals and Interferences based upon the same record must be filed within one month from the date hereof (37 CFR 1.197).

With respect to the new rejection under 37 CFR 1.196(b), should appellant elect the alternate option under that rule to prosecute further before the Primary Examiner by way of amendment or showing of facts, or both, not previously of record, a shortened statutory period for making such response is hereby set to expire two months from the date of this decision. In the

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event appellant elects this alternate option, in order to preserve the right to seek review under 35 U.S.C. 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If the appellant elects prosecution before the examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to us for final action on the affirmed rejection, including any timely request for reconsideration thereof.

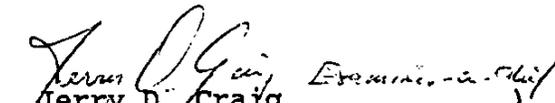
No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR 1.136(a). See the final rule notice, 54 F.R. 29548 (July 13, 1989), 1105 O.G. 5 (August 1, 1989).

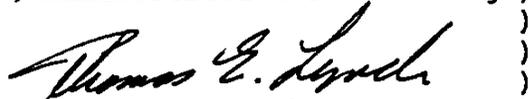
Effective August 20, 1989, 37 CFR 1.196(b) has been amended to provide that a new ground of rejection pursuant to the rule is not considered final for the purpose of judicial review under 35 U.S.C. 141 or 145.

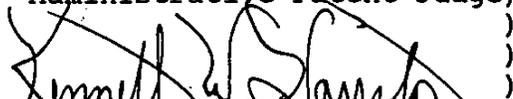
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Failure by appellants to timely request reconsideration by the Board or to timely seek prosecution before the examiner with respect to the new rejection as provided for by 37 CFR 1.196(b) will result in the cancellation of all the claims subject to the new rejection.

AFFIRMED-IN-PART  
37 CFR 1.196(b)

  
Jerry D. Craig  
Administrative Patent Judge

  
Thomas E. Lynch  
Administrative Patent Judge

  
Kenneth W. Hairston  
Administrative Patent Judge

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