

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 38

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES L. PATERSON and
GREGORY J. ARMSTRONG

Appeal No. 94-3910
Application No. 07/966,615¹

ON BRIEF

Before THOMAS, HAIRSTON and JERRY SMITH, Administrative Patent Judges.

¹ Application for patent filed October 26, 1992. According to appellants, the application is a continuation of Application 07/707,242, filed May 22, 1991, now abandoned; which is a continuation of Application 07/526,961, filed May 22, 1990, now abandoned; which is a continuation of 07/128,549, filed December 3, 1987, now abandoned.

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JERRY SMITH, Administrative Patent Judge.

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DECISION ON APPEAL

BACKGROUND

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 21-28, which constitute all the claims remaining in the application. Claims 22-28 ultimately depend from claim 21.

The invention pertains to Erasable Programmable Read Only Memory (EPROM) semiconductor devices and their fabrication.

Independent claim 21 is reproduced as follows:

21. An array of rows and columns of memory cells comprising:

a substrate having a first conductivity type;

a plurality of source/drain regions formed in the surface of said substrate, said source/drain regions having a second conductivity type opposite said first conductivity type and said source/drain regions extending at least between two adjacent rows of memory cells of said array;

a plurality of field insulating regions formed on a portion of the surfaces of said source/drain regions;

a plurality of slots etched in said field insulating regions, said slots exposing the surface of said source/drain regions and extending the length of said source/drain regions and extending at least between two adjacent rows of memory cells of said array;

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a first plurality of conductive layers formed directly on and extending the length of the exposed portion of said source/drain regions;

a plurality of insulating layers formed on the surface of said conductive layer; and

a plurality of gates controlling conductivity between said source/drain regions.

The examiner relies on the following references:

Sugiura et al. (Sugiura)	4,451,904	May 29, 1984
Takasaki et al. (Takasaki)	4,581,622	Apr. 8, 1986
Esquivel et al. (Esquivel)	4,833,514	May 23, 1989 (filed Nov. 18, 1987)

Rather than repeat the arguments of appellants or the examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the reasons relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the brief along with the examiner's

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rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

The rejection of Claim 28 under 35 U.S.C. § 112

Claim 28 stands rejected under 35 U.S.C. § 112, first paragraph, because the specification allegedly does not provide support for "a second plurality of conductive layers . . . in electrical contact with said first plurality of conductive layers" [answer, page 3]. We reverse this rejection.

Appellants argue the specification teaches that the embodiment shown in Figure 2G, when combined with the embodiment shown in Figures 5A-5F, teaches "a second plurality of conductive layers" [brief, pages 4-5]. The examiner argues that the specification does not teach the combination argued by appellants. The examiner does not dispute that the combination asserted by appellants would teach a "second plurality of conductive layers."

The specification as filed states, with respect to Figure 4 which features conductors 16, 17 and 18, that the resistance of source/drain regions 7, 8 and 9 "may be lower if a particular conductive region is incorporated as discussed

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below" [specification, page 15, lines 16-20] (emphasis added).

Later, the specification states:

As discussed above, the present invention additionally contemplates an embodiment which uses conductive regions immediately overlying N++ regions 7, 8, and 9. . . . Figures 5A through 5F illustrate a procedure which a preferred embodiment utilizes to form these conductive regions, which consist of buried silicide layers [Id. at 17, lines 11-18] (emphasis added).

Thus, the specification clearly teaches the use of conductors 16, 17 and 18 with the embodiment shown in Figures 5A-5F. Therefore, the originally filed disclosure supports the invention of claim 28. Accordingly, we reverse this rejection of claim 28.

The rejection of Claims 21-28 under 35 U.S.C. § 112

Claims 21-28 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which appellants regard as the invention. We reverse this rejection.

The rejection of claims 21-28 under § 112 is based on the examiner's misunderstanding of the use of the phrase

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"extending the length" in two places of independent claim 21 from which the remaining claims ultimately depend. Lines 9-10 of claim 21 read in relevant part, "said slots . . . extending the length of said source/drain regions," and line 12 reads in relevant part, "a first plurality of conductive layers . . . extending the length of the exposed portion of said source/drain regions." The examiner reads these sections as indicating, respectively, that the slots cause the source/drain regions to become longer and the conductive layers cause the exposed portion to become longer. The correct and sufficiently clear meaning of these quoted sections is that, respectively, the slots are at least as long as the source/drain regions, and the conductive layers are at least as long as the exposed portion of said source/drain regions. The artisan would have no difficulty understanding the scope of these claims in view of the specification. Accordingly, we reverse this rejection of claims 21-28.

The rejection of Claims 21-28 under 35 U.S.C. § 103

Claims 21-28 stand rejected under 35 U.S.C. § 103. Claims 21-23 and 25-28 are rejected under § 103 as obvious over Sugiura in view of Takasaki. Claim 24 is rejected under

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§ 103 as obvious over Sugiura and Takasaki and further in view of Esquivel. As explained more fully below, it appears to us that the examiner did not understand certain elements of independent claim 21. Under the reasoning of In re Steele, 305 F.2d 859, 862, 134 USPQ 292, 295 (CCPA 1962), we are constrained to reverse the rejection of independent claim 21 under § 103 since the examiner admittedly did not understand elements of the claim which we determine to be essential to applying the cited art to claim 21. The examiner's failure to properly identify the limitations of claim 21 and the examiner's failure to respond to appellants' arguments regarding the merits of the prior art rejection force us to conclude that the examiner has failed to establish a prima facie case of the obviousness of claim 21. Since we reverse the rejection as to Claim 21, we reverse the rejection of claims 22-28 all of which ultimately depend from claim 21.

Appellants argue, inter alia, that Sugiura does not disclose "a plurality of slots etched in said field insulating regions, said slots exposing the surface of said source/drain regions and extending the length of said source/drain regions and extending at least between two adjacent rows of memory

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cells of said array." The examiner cites generally that Sugiura teaches the claimed slots and notes elements 39a and 39 of Sugiura.

Sugiura teaches etching a gap in the field insulating region 34 to form contact holes 39 "which expose the surface portion of the Si substrate to the outside" [column 9, lines 52-56; Figure 11]. It appears from Figure 11 that Sugiura may expose some portion of B2 which the examiner asserts is a source/drain region. Presuming for the moment that Sugiura teaches "a plurality of slots etched in said field insulating regions, said slots exposing the surface of said source/drain regions," it remains unclear whether the contact holes extend (a) "the length of said source/drain regions," and (b) "at least between two adjacent rows of memory cells of said array" as recited in claim 21. Appellants specifically argue these limitations in the brief, and the examiner fails to respond on the ground that the claims are indefinite. Specifically, it appears fairly clear that the examiner did not understand what was meant by the phrase "extending the length" as is evidenced by his rejection of claim 21 under 35 U.S.C. § 112, second paragraph addressed above. Moreover, the only argument

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offered by the examiner in his answer to appellants' arguments that Sugiura does not disclose the claimed slots is as follows:

Since the nature of the claim language can not be determined, the rejection under 35 USC 103 may be properly applicable to the claims once they are definite within the meaning of 35 USC 112 [answer, page 7] (emphasis added).

Since it is essential in applying the prior art to independent claim 21 that one understands the meaning of the claim language, and since the examiner admittedly did not understand some of the recitations of claim 21, we are constrained to hold that the examiner has failed to properly establish a prima facie case of obviousness. Accordingly, we reverse the § 103 rejection of claim 21 and the rejection of claims 22-28 which ultimately depend from claim 21.

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In summary, we have reversed each of the examiner's rejections of the claims. Therefore, the decision of the examiner rejecting claims 21-28 is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
KENNETH W. HAIRSTON)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
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JERRY SMITH)	
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LP

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Draft Final

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