

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEPHEN A. HUCKSTEPP

Appeal No. 94-4061
Application 07/659,683¹

ON BRIEF

Before SCHAFER, Vice-Chief Administrative Patent Judge, and
HAIRSTON and CRAWFORD, Administrative Patent Judges.

CRAWFORD, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed February 25, 1991.

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This is a decision on an appeal² from the examiner's final rejection³ of claims 3-7, 9, 12, 13, 15 and 16. Claims 1, 2, 8, 10, 11 and 14 have been canceled. Appellant's appealed subject matter is a microprocessor apparatus and a method of supervising a microprocessor which include watchdog circuit means connected to the output lines of the microprocessor for resetting the microprocessor if an error in the sequence of processing the program steps is detected. Claims 9 and 15 are illustrative of the claims on appeal and recite:

9. A microprocessor apparatus comprising:

microprocessor means for executing a predetermined program which includes a plurality of watchdog instructions which are different from one another and all of which would be executed during complete execution of said program wherein a first watchdog instruction is located in a main loop of said program and a second watchdog instruction is located in a sub-routine that is non-conditionally called for during execution of said main loop;

watchdog instruction decoder means connected to an output of said microprocessor means for decoding a signal supplied at said output in response to execution of each watchdog instruction including each of the first and second watchdog instructions to provide a respective one of a plurality of activation signals on one of a plurality of output lines thereof such that, if said microprocessor means is operating correctly, said output lines will be provided with said activation signals in a predetermined sequence; and

² Notice of Appeal filed November 22, 1993.

³ Office Action mailed May 18, 1993.

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watchdog circuit means connected to said output lines for resetting said microprocessor means in response to an occurrence of said activation signals on said output lines in other than said predetermined sequence.

15. A method of supervising the operation of a microprocessor, said method comprising the steps of:

including in a program executed by said microprocessor a plurality of watchdog instructions which are different from one another and all of which would be executed during complete execution of said program, wherein said program includes a first watchdog instruction in a main loop of said program and a second watchdog instruction in a sub-routine that is non-conditionally called for during execution of said main loop;

initiating execution of said program by said microprocessor;

decoding an output of said microprocessor to produce a respective one of a plurality of activation signals at a corresponding one of a plurality of signal terminals on execution of a respective watchdog instruction such that, if said microprocessor is operating correctly according to said program, said activation signals will be provided at respective ones of said plurality of signal terminals in a predetermined sequence; and

resetting said microprocessor if said activation signals are provided at said plurality of signal terminals other than in said predetermined sequence.

Claims 3, 4, 5, 9, 12, 13 and 15 stand or fall together. Claims 7 and 16 stand or fall together and claim 6 stands alone (Brief at page 7).

THE REFERENCES

Proto	4,108,359	Aug. 22, 1978
Owens	4,594,685	Jun. 10, 1986
Gercekci	4,763,296	Aug. 9, 1988

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THE REJECTIONS

Claims 3-7, 9, 12, 13, 15 and 16 stand rejected under 35 U.S.C. § 112, second paragraph, as being "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention" (Examiner's Answer, page 3). Claims 3-7, 9, 12, 13, 15 and 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Owens (Examiner's Answer, page 4). Claims 3-7, 9, 12, 13, 15 and 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Gercekci and Proto (Examiner's Answer, page 5).

Rather than reiterate the examiner's full statement of the above-noted rejections and the conflicting viewpoints advanced by the appellant and the examiner regarding those rejections, we make reference to the examiner's answer (Paper No. 15) and the appellant's brief (Paper No. 14) and reply brief (Paper No. 16) for the full exposition thereof.

OPINION

In reaching our conclusions on the issues raised in this appeal, we have carefully considered appellant's specification, the claims, the applicable law, the applied references and the respective viewpoints advanced by the appellant and the examiner. As a consequence of our review, we

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have made the determination that the examiner's rejections of claims 3-7, 9, 12, 13, 15 and 16 should not be sustained. Our reasons for the determination follow.

With regard to the examiner's rejection of claims 3-7, 9, 12, 13, 15 and 16 under 35 U.S.C. § 112, second paragraph, we initially note that the purpose of the requirement stated in the second paragraph of 35 U.S.C. § 112 is to provide those who would endeavor, in future enterprise, to approach the area as circumscribed by the claims of a patent, with the adequate notice demanded by due process of law, so that they may more readily and adequately determine the boundaries of protection involved and evaluate the possibility of infringement and dominance. In re Hammack, 427 F.2d 1378, 1382, 166 USPQ 204, 208 (CCPA 1970). The inquiry as stated in In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971) is:

... whether the claims do, in fact, set out and circumscribe a particular area with a reasonable

degree of precision and particularity.... [t]he definiteness of the language employed must be analyzed--not in a vacuum, but always in light of the teachings of the prior art and of the particular

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application disclosure as it would be interpreted by one possessing the ordinary level of skill in the pertinent art.

In the instant case, the examiner is of the opinion that the use of the term "watchdog instruction decoder" is a misnomer, because the address decoder 16 does not decode watchdog instructions. The appellant counters:

In comprehending the import of this language, a person of ordinary skill in the art would also resort to the specification which, in one embodiment, regards certain addresses output by a microprocessor as watchdog instructions. See, for example, lines 14-19 on page 7 and lines 4-6 on page 9. In the disclosed embodiment, when each address constituting a watchdog instruction is received on the address bus 14 of Fig. 1, the decoder 16 decodes the address as a watchdog instruction and provides an activation signal on one of the lines L1 through L4 of the decoder 16. Accordingly, the execution of each watchdog instruction is the provision of the address on the address bus 14 in response to which the address decoder 16, acting as a watchdog instruction decoding means, decodes the watchdog instruction (that is, the address) to provide a respective one of a plurality of activation signals on one of a plurality of output lines, as recited in claim 9. [Brief at page 9]

We are in agreement with appellant and note further that the term "watchdog decoder" in claim 9 need not comport with the strict meaning of a "decoder" because an appellant may be his own lexicographer as long as the words in the claims are clear. See, e.g., Jonsson v. Stanley Works, 903 F.2d 812, 821, 14 USPQ2d 1863, 1871 (Fed. Cir. 1990).

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As to claim 6, the examiner states that it is not clear what role the recirculating shift register means has within the scheme of the invention.

Appellant's specification discloses that the shift register 28 is initially loaded by initializing circuit 46 with a logic pattern 1,0,0,0 so that the output of latches 44.1, 44.2, 44.3 and 44.4 depicted in Figure 1 are set at 1,0,0,0 (Specification, page 8). The respective outputs of the latches 44.1 to 44.4 are connected to one input of one of AND gates 30.1, 30.2, 30.3 and 30.4. The other input of the AND gates is connected to the output lines L1, L2, L3, and L4 from address decoder 16. (Specification, page 8, Figure 1). The specification also teaches that if the logic pattern on L1, L2, L3, L4 is 1,0,0,0:

the outputs of the AND-gates 30.1 to 30.4 go to levels 1,0,0 and 0, respectively (since both inputs of the gate 30.1 are at level 1, whereas the two inputs of each of the gates 30.2 to 30.4 are at level 0). Consequently, the output of the OR-gate 32 goes active (goes to level 1) and the counter 26 is reset to zero. [Specification, page 9]

The specification also discloses that if the logic pattern on lines L1, L2, L3 and L4 does not match the logic pattern output from latches 44.1, 44.2, 44.3 and 44.4:

the mismatch between the bit pattern on the lines L1 to L4 and the pattern outputted by the shift register will

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result in none of the AND-gates 30.1 to 30.4 having both of its inputs at level 1. Consequently, the output of the OR-gate 32 will remain at level 0 whereby the output of the inverter will remain at level 1. Thus, both inputs of the AND-gate 40 will be at level 1 (active) whereby the output of the gate 40 will go to level 1 and this level will be passed to the reset input RS of the microprocessor 10, via the OR-gate 42, so as to reset the micro-processor.
[Specification, pages 11-12]

This relationship between the shift register and the output lines of the microprocessor is also recited in the claims. Claim 3, which is dependent on claim 9, recites that the microprocessor apparatus comprises a "logic means for applying a reset command to a reset input of said microprocessor means in response to the occurrence of said activation signals on said plurality of output lines other than in said predetermined sequence." Claim 6, which is dependent on claim 3, recites that the logic means comprises a "recirculating shift register means" and a "plurality of AND function means" which produce a:

"predetermined logic signal at an output thereof upon the provision of a predetermined logic signal at each of a respective one of said output lines and a respective stage of said shift register."

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We are of the opinion that the language of the claims clearly recites the role of the recirculating shift register means especially when viewed in light of the specification.

The examiner is of the view that the language: 'for decoding said predetermined address upon the execution of a corresponding watchdog instruction' in claim 7 would be more accurate if "upon" is replaced by "subsequent to" because decoding addresses of watchdog instructions and execution of watchdog instruction cannot occur at the same time (Examiner's Answer, pages 3 and 7). We do not agree with the examiner that the term "upon" in claim 7 indicates that the decoding and execution steps occur at the same time. The ordinary meaning of the term "upon" is "immediately following or very soon after."⁴

As to claim 15, the examiner states that the term "including" is an abstract term that does not describe physical operation. In our view, the person of ordinary skill in the art would understand that a plurality of watchdog instructions are included in a program executed by a microprocessor. In any event, we agree with the appellant that the term "including" is generally understood to mean "to place, list, or rate as a part

⁴ Webster's Third New International Dictionary (G.&C. Merriam Co. 1981).

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or component of a whole or of a larger group, class or aggregate⁵" and thus connotes a physical step. We also agree with the appellant that loading instructions in the form of data in a memory normally involves applying voltages to pins of one or more integrated circuit memories in order to store electric charge in certain electrical components within the circuits of the memory IC's and thus is a physical step.

The examiner further states that the language: 'decoding an output of said microprocessor to produce a respective ... signals... on execution of a respective watchdog instruction' recited in claim 15 does not fully recite the nature of 'output' generated as a result of the execution (Examiner's Answer, page 3). The examiner explains that 'an output' is too broad to define the type of signal, because there are so many different signals output from a microprocessor and that 'on execution' is recited in an ambiguous way, because it is not clear what executes the watchdog instruction (Examiner's Answer, page 8). The examiner may be correct that the language "an output" is broad, but just because language in a claim is broad

⁵ Webster's Third New International Dictionary (G.&C. Merriam Co. 1981).

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does not mean that it is indefinite See In re Miller, 441 F.2d 689, 693, 169 USPQ 597, 600 (CCPA 1971).

We are not in agreement with the examiner that it is not clear what executes the watchdog instruction. Claim 15 recites "including in a program executed by said microprocessor a plurality of watchdog instruction" and "initiating execution of said program by said microprocessor." In addition, the specification states at page 3, lines 7-8 "a microprocessor arrangement which includes a microprocessor that executes a program which includes a number of watchdog instructions." In view of the language of claim 15 and the teachings in appellant's specification, we are of the opinion that persons of ordinary skill in the art would clearly understand that it is the microprocessor which executes the watchdog instructions.

We also disagree with the examiner when he states that the language: 'resetting said microprocessor means in response to an occurrence of said activation signals... in other than said predetermined sequence' recited in claim 9 and similarly recited in claim 15 does not precisely recite when the resetting occurs (Examiner's Answer, Page 3). In our view, it is clear from the language of claims 9 and 15 that the microprocessor is reset when the activation signals occur out of sequence. This is also

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disclosed quite clearly in appellant's specification
(Specification, page 11, line 26 to page 12, line 11).

In view of the foregoing, we will not sustain the
examiner's rejection of claims 3-7, 9, 12, 13, 15 and 16 under 35
U.S.C. § 112, second paragraph.

In regard to the rejections of claims 3-7, 9, 12, 13,
15 and 16 under 35 U.S.C. § 103, the examiner bears the initial
burden of presenting a prima facie case of obviousness. In re
Rijckaert, 9F.3d 1531, 1532, 28 USPQ 2d 1955, 1956 (Fed. Cir.
1993); In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ 1443, 1444
(Fed. Cir. 1992). Only if the burden is met does the burden of
coming forward with evidence or argument shift to the applicant.
Id. If the examiner fails to establish a prima facie case, the
rejection is improper and will be overturned. In re Fine, 837
F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Turning first to the rejection under 35 U.S.C. § 103 of
claims 3-7, 9, 12, 13, 15 and 16 in view of Owens, we find that
Owens discloses a processor 10 with outputs at terminals BIT 1
and BIT 2 (Figure 1). A timer circuit 20, 25 is connected to the
output of BIT 2 and a bit pattern manipulator 15 is connected to
terminals BIT 2.

The output of BIT 2 is a clocking signal and is connected to shift register 20. The pattern stored in the shift register 20 is reloaded each time a clocking signal is output at BIT 2 and as a result shift register 20 sends a high signal to counter 25 which clears the counter (Col. 6, lines 6-13). If the clocking signal is not output from BIT 2 at a sufficient rate, the counter will count up and expire (Col 6, lines 18-23). If the counter expires, a signal will pass to OR gate 18 which will thus reset processor 10 (Col. 6, lines 44-48).

The bit pattern manipulator includes a shift register 15 which is a recirculating shift register which is initially loaded with a predetermined bit pattern (Col. 8, lines 7-14). When a watchdog instruction is received and decoded by the processor 10, the signal output at BIT 2 is set to low (Col. 7, lines 26-39). In addition, the bit pattern at BIT 1 is set to coincide with a specific predetermined masked bit (most significant bit) of the bit pattern stored in a first register AL of processor 10 (Col. 7, lines 33-39). The bit pattern in AL is then manipulated. In the embodiment disclosed in Owens, the bit pattern is shifted to the right (Col. 7, lines 41-46). BIT 2 is then set to high and outputs a clocking signal to shift register 15 which causes shift register 15 to shift the stored bit pattern

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one place to the right so that one bit (most significant bit) is shifted off and recirculated and also applied to NOR gate 16 (Col. 8, lines 13-15). NOR gate 16 is also coupled to BIT 1 (whose bit pattern has also been shifted to the right) (Col. 8, lines 16-19). If the two inputs to NOR gate 16 are not the same, NOR gate 16 is enabled (Col. 8, lines 18-20). The NOR gate 16 together with the clocking signal enables AND gate 17 and the processor 10 is reset (Col. 8, lines 19-21). As long as the processor 10 is operating in a predetermined sequence which corresponds to the bit pattern stored in shift register 15 and the counter has not counted up, the processor 10 will not be reset.

Recognizing that Owens does not disclose a "watchdog instruction decoder means connected to an output of said microprocessor means" as recited in claim 9, the examiner states:

whether the decoder lies inside or outside the microprocessor is not critical to the invention as long as the means properly function as a detector of a watchdog instruction and any means including a software CALL ROUTINE execution means inside a microprocessor, that detects the watchdog instruction and generates activation signals, would be equivalent [Examiner's Answer, page 9, emphasis added].

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We do not agree with the examiner, that any means that detects watchdog instructions is equivalent to the means disclosed in the specification. Our reviewing court in In re Bond, 910 F2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990) has stated:

While a "means-plus-function" limitation may appear to include all means capable of achieving the desired function, the statute requires that it be "construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof" (emphasis in original).

A factor to consider in the determination of whether a prior art element is an equivalent of the claimed element is whether the prior art element performs the function in the claim in substantially the same manner as the function is performed by the corresponding element described in the specification i.e. whether the prior art element is a structural equivalent of the claimed element. Id. at 834, 15 USPQ2d at 1568.

In the instant case, appellant's claimed watchdog decoder means is address decoder 16 which is depicted in Figure 1. Appellant discloses that address decoder 16 receives address portions of each instruction executed by the microprocessor (Page 7, lines 11-14). Address decoder 16 does not respond to addresses which do not result from the execution of watchdog instructions (Page 7, lines 20-22). However, when address

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decoder 16 detects a watchdog instruction, it activates one of a plurality of output lines L1 to L4 (Page 7, lines 22-24).

Appellant's specification also discloses that each of the watchdog instructions is different and that address decoder 16 activates one of the output lines L1 to L4 in response to the watchdog instruction (Page 7, lines 24-25).

Owens does not disclose that the watchdog instructions are decoded by detecting an address portion of an instruction and responding to instructions which are watchdog instructions by activating a plurality of output lines depending on the watchdog instruction received. In contrast, each time a watchdog instruction is decoded, BIT 1 is activated and BIT 2 is deactivated. There is no basis for finding that Owens discloses an equivalent of the watchdog decoder structure disclosed in appellant's specification. In addition, the examiner has not articulated any motivation for placing the decoder outside of the microprocessor. Nor has the examiner provided any factual basis for concluding that the location of the decoder is not critical. In view of the foregoing, we will not sustain the rejection of claims 3-7, 9, 12, 13, 15 and 16 under 35 U.S.C. § 103 as being unpatentable over Owens.

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Turning next to the rejection of claims 3-7, 9, 12, 13, 15 and 16 under 35 U.S.C. § 103 over Gercekci and Proto, we find that Gercekci discloses a processor 2 having a first memory 4 which holds the primary operating routine of the microprocessor (Col. 2, lines 27-29). The operating routine includes predetermined addresses for instructions to reset a timer 10 (Col. 2, lines 31-33). In order to prevent false resetting of the timer 10, a watchdog timer 8 is provided which includes a second memory 12 which stores the predetermined addresses and a comparator 18 which compares the address of each reset instruction with the addresses stored in second memory 12 (Col. 3, lines 7-11). If the addresses coincide, comparator 16 outputs a signal to AND gate 22 which together with the RTR (reset timer request) signal is enabled and the timer is reset (Col. 3, lines 8-12). Gercekci discloses that if the reset instruction is located at an address other than the next predetermined address, the AND gate would not be enabled and therefore would not produce a signal to reset the timer (Col. 3, lines 35-48).

The examiner, recognizing that Gercekci does not disclose a decoder that generates activation signals that are input to shift register means, relies on Proto for teaching a method of using shift registers updated by activation signals

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(21) to determine the validity of a sequence of instructions executed (Examiner's Answer, pages 5-6).

We find that Proto discloses an apparatus for verifying the execution of a sequence of coded instructions which includes a processor 10, a memory 11 and a sequence error detector 20 (Fig. 1). Sequence error detector 20 monitors the sequence of instructions stored in memory 11 through lines 15 from which processor 10 reads instructions from memory 11 (Fig. 1, Col. 3, lines 51-53). Sequence error detector 20 includes a reference checkword storage 31, a comparator 32, and shift register 37 having stages R_1 , R_2 etc. Shift register 37 along with adders 40 modify the binary sequence received from the processor and form a checkword which is sent to comparator 32 which compares the checkword received from stages R_1 , R_2 etc. and adders 40 with the reference checkword provided from reference checkword storage 31 (Col. 4, line 49-Col 5, line 21). If the two words are not the same, indicating that the instructions from processor 10 are out of sequence, the comparator outputs a signal which indicates that there is an error (Col. 4, lines 9-13, Col. 5, lines 23-25).

The examiner stated:

It would have been obvious to a person of ordinary skill in the art at the time the invention was made that the means of checking valid sequence of

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instruction execution in Proto is an alternate design to the means of checking valid sequence of instruction execution in Gercekci and the person would have implemented either means as an equivalent option depending on the inter-facing constraints imposed by other means of the system. [Examiner's

Answer, Page 6]

As the watchdog instruction decoder is recited in claim 9 in means-plus-function format, we must look to the specification and construe the "means" language so as to be limited to the corresponding structure disclosed in the specification and equivalents thereof. In re Donaldson 16 F.3d 1189, 1195, 29 USPQ2d 1845, 1850 (Fed. Cir. 1994).

Appellant's disclosed watchdog instruction decoder means is an address decoder 16 which receives an address portion of each instruction executed in memory and activates one of lines L1, L2, L3, L4 in response to detecting an address of a watchdog instruction. Proto discloses no such address decoder. Even if we accept the examiner's rationale that the decoder in Proto is within memory device (11) (Examiner's Answer, page 10), there is no disclosure of an address decoder as disclosed in the specification or an equivalent thereof. In view of the foregoing, we will not sustain the examiner's rejections of

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claims 3-7, 9, 12, 13, 15 and 16 under 35 U.S.C. § 103 as being unpatentable over Gercekci and Proto.

The examiner's decision is reversed.

REVERSED

RICHARD E. SCHAFER, Vice)	
Administrative Patent Judge)	
)	
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)	
KENNETH W. HAIRSTON)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
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Appeal No. 94-1379
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