

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 11

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DONALD L. PLUMTON and HAN-TZONG YUAN

Appeal No. 95-0347
Application 08/056,681¹

ON BRIEF

Before URYNOWICZ, LEE and CARMICHAEL, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1, 2, 4, 5, 7, 12 and 13. Claims 16-19 have been withdrawn from consideration, and claims 3, 6, 8-11, 14 and 15 have been objected to as being dependent on a rejected claim. No claim has been allowed.

¹ Application for patent filed April 30, 1993.

Appeal No. 95-0347
Application 08/056,681

Reference relied on by the Examiner

Muraoka 4,654,679 Mar. 31, 1987

The Rejections on Appeal

Claims 1, 2, 4, 5, 7, 12 and 13 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by Muraoka.

The appellants have grouped all rejected claims together as standing and falling with independent claim 1. (Br. at 2).

Claim 13, as amended in Paper No. 4, no longer depends from claim 11 as is reproduced in the appellants' Appendix filed with the appeal brief, but depends from claim 12 instead.

The Invention

The invention is directed to a field effect transistor wherein the gate has a varying doping level where it abuts the channel region in the direction from the source region to the drain region. Claim 1 is the only independent claim on appeal in the application and is reproduced below:

1. A field effect transistor, comprising:
 - (a) a source region in a semiconductor layer;
 - (b) a drain region in said semiconductor layer;
 - (c) a gate region in said semiconductor layer and between said source region and said drain region;

Appeal No. 95-0347
Application 08/056,681

(d) a channel region in said semiconductor layer and between said source region and said drain region and abutting said gate region;

(d) wherein said gate region has a doping level where said gate region abuts said channel region varying in the direction from said source region to said drain region.

The recitation of two steps labeled "d" should be corrected when this case returns to the jurisdiction of the examiner.

Opinion

We do not sustain the rejection of claims 1, 2, 4, 5, 7, 12 and 13 as being anticipated by Muraoka.

Anticipation is established only when a single prior art reference discloses, either expressly or under the principles of inherency, each and every element of the claimed invention. In re Spada, 911 F.2d 705, 707, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed.Cir. 1984). See also In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986); Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). The prior art reference must either expressly or inherently describe each and every limitation in a claim. Verdegaal Bros. v. Union

Appeal No. 95-0347
Application 08/056,681

Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir.),
cert. denied, 484 U.S. 827 (1987).

Moreover, the examiner has the initial burden of establishing prima facie anticipation by coming forward with evidence tending to disprove novelty. In re Wilder, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). A prima facie case means the evidence of prior art would reasonably allow the conclusion the examiner seeks and compels such a conclusion if the applicant produces no evidence or argument to rebut it. In re Spada, 911 F.2d at 707 n.3, 15 USPQ2d at 1657 n.3 (Fed. Cir. 1990).

We agree with the appellants that the examiner has not established prima facie anticipation.

The claims recite a field effect transistor, not a thyristor. A thyristor is a semiconductor device having at least three junctions (The New IEEE Standard Dictionary of Electrical and Electronic Terms, Fifth Ed., 1993, at page 1372 / page attached), and should not be confused with a field effect transistor (Semiconductor Devices, Heathkit-Zenith Educational Systems, 1978, at page 8-3 / page attached). The examiner does

Appeal No. 95-0347
Application 08/056,681

not dispute the appellants' assertion that Muraoka discloses a thyristor and that a thyristor is not a field effect transistor. Rather, the examiner points to an equivalent circuit to Muraoka's thyristor which **includes** a field effect transistor.

The equivalent circuit relied on by the examiner is shown in Muraoka's Figure 2 and includes a junction field effect transistor T2 connected to a p-n-p bipolar transistor T1. Specifically, the drain of the field effect transistor T2 is connected to the base of the bipolar transistor T1. A first terminal 9 is connected to the source of the field effect transistor; a second terminal is connected to the emitter of the bipolar transistor, and a third terminal is connected to the gate of the field effect transistor.

The examiner's position is misplaced and does not adequately support the anticipation rejection. The multi-component equivalent circuit shown in Muraoka's Figure 2 is merely a functional equivalent. There is no disclosure as to the internal structure of the field effect transistor component T2 in the equivalent circuit. The internal structure of the field effect transistor T2 shown in Figure 2 is not disclosed. The examiner has articulated no reasonable basis to read Muraoka's description

Appeal No. 95-0347
Application 08/056,681

of characteristic features directed to the **thyristor** as if it were description for a **transistor component** in a functionally equivalent circuit to the **thyristor**. Figure 3 of Muraoka shows another equivalent circuit to a thyristor. Similarly, the examiner has set forth no basis to regard description for the

gate of the thyristor as if it is for the gate of a transistor component in an equivalent circuit. To assume that to be the case is highly speculative and without adequate basis on this record.

The examiner states (answer at 4) that Muraoka's Figure 9 [10] shows gate regions between source and drain regions and channel regions next to the gate regions, which are typical of field effect transistor structure. However, in Muraoka the cited regions are not connected for operation as a field effect transistor. They are only a portion of the disclosed thyristor and do not have independent significance in the Muraoka disclosure as an operative field effect transistor, while the appellants specifically claim a field effect transistor. This difference alone is sufficient to undermine a rejection for anticipation.

Appeal No. 95-0347
Application 08/056,681

For the foregoing reasons, the rejection of independent claim 1 cannot be sustained. The rejection of all claims depending directly or indirectly from claim 1 also cannot be sustained.

Conclusion

The rejection of claims 1, 2, 4, 5, 7, 12 and 13 under 35 U.S.C. § 102(b) as being anticipated by Muraoka is reversed.

REVERSED

STANLEY M. URYNOWICZ)
Administrative Patent Judge)
)
)
) BOARD OF PATENT
JAMESON LEE)
Administrative Patent Judge) APPEALS AND
)
) INTERFERENCES

Appeal No. 95-0347
Application 08/056,681

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Appeal No. 95-0347
Application 08/056,681

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