

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JUNICHI SATO
and TETSUO GOCHO

Appeal No. 95-1009
Application 07/858,632¹

ON BRIEF

Before KIMLIN, PAK and WALTZ, ***Administrative Patent Judges.***

WALTZ, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1 through 6, which are all the claims in this application.

According to appellants, the invention is directed to a

¹ Application for patent filed March 27, 1992.

Appeal No. 95-1009
Application 07/858,632

method of fabricating semiconductor devices having grooves or trenches in the surface of a substrate which are filled up with a filling material by a bias ECR-CVD process and then leveled (main brief, page 1).

Appellants state that the claims do not stand or fall together (main brief, page 2) and present specific reasons for the separate patentability of each claim on pages 2-5 of the main brief. See 37 CFR § 1.192(c)(5)(1993). A copy of claims 1 through 6 taken from appellants' brief is appended to this decision.

The following references have been relied upon by the examiner:

Kaanta et al. (Kaanta)	4,793,895	Dec. 27, 1988
Olmer	5,089,442	Feb. 18, 1992

Wolf, *Silicon Processing for the VLSI Era*, Volume 2: Process Integration, pp. 237-239 and 285-286 (Lattice Press, 1990)

Claims 1 and 3 stand rejected under 35 U.S.C. § 102(b) as anticipated by Wolf. Claims 1, 2, 4 and 5 stand rejected under 35 U.S.C. § 102(b) as anticipated by the admitted prior art. Claim 6 stands rejected under 35 U.S.C. § 102(b) as

Appeal No. 95-1009
Application 07/858,632

anticipated by Kaanta.² Claims 1, 2 and 4 stand rejected under 35 U.S.C.

§ 103 as unpatentable over Olmer. We *affirm* the stated rejections over Wolf, Kaanta and Olmer. We *affirm* the stated rejection of claims 1 and 4 over the admitted prior art but reverse the rejection of claims 2 and 5 over the admitted prior art.

Pursuant to our authority under 37 CFR § 1.196(b), we enter a new ground of rejection of claim 5 under 35 U.S.C. § 103 as unpatentable over Olmer.

DECISION

A. The Rejection in view of Wolf

The method of appealed claim 1 requires, in a method where grooves formed in a substrate are filled up with a filling material deposited by a process in which etching and deposition are achieved concurrently, the improvement comprising (1) leveling of the height of portions of the filling material deposited on portions of the substrate other

² The final rejection of claim 6 under § 102(b) was over Kaanta or Lasky (U.S. Patent No. 4,735,679). However, the examiner withdrew Lasky as being "cumulative" (answer, page 2).

Appeal No. 95-1009
Application 07/858,632

than the grooves; and (2) polishing away said portions of the filling material to smooth the entire substrate surface.

Claim 3 further limits the method of claim 1 in reciting that the leveling is achieved by a full surface etch back process.

For a proper rejection under § 102, every limitation of a claim must identically appear in a single prior art reference for it to anticipate the claim. See *In re Bond*, 910 F.2d 831, 832, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990). Wolf describes the deposition of a filler material such as SiO₂ in a groove of a substrate by ECR-CVD (which is a method in which etching and deposition are achieved concurrently, see the specification, page 3, lines 11-16, and Wolf, page 237). Wolf teaches that this deposition process partially planarizes the surface and resist etchback is used to completely planarize (i.e., level) the surface (see page 285). CMP (chemical mechanical polishing) is then employed to polish the surface in order to remove the oxide spikes formed by the etchback conditions (Wolf, page 238). Wolf clearly emphasizes the use of etchback planarization in combination with CMP (page 238). Therefore every limitation of claims 1 and 3 is described by

Wolf within the meaning of § 102.

Appellants argue that Wolf only teaches the polishing of small elevated features (i.e., spikes) and this is very different from polishing the entire surface as recited in the method of claim 1 (brief, page 2). However, appellants' argument is not well taken since Wolf teaches that the CMP process can remove such small elevated features "without significantly thinning the oxide on the flat areas." (page 238). It is clear from this passage that the CMP of Wolf is accomplished across the entire wafer or substrate. Wolf further evinces that polishing is across the entire wafer on page 239 where Wolf notes that a problem is "maintaining sufficient polishing-rate uniformity across the wafer" (see the answer, page 5).

B. The Rejection in view of the admitted prior art

The scope of claim 1 has been discussed above. Claim 2 further limits the method of claim 1 by requiring the "leveling" to be achieved by an additional deposition of the filling material. Claims 4 and 5 are independent claims with

the same Jepson-type preamble³ as claim 1. Claim 4 states that the improvement comprises effecting the deposition process such that the differences in thickness between a central portion and a peripheral portion are canceled out, followed by polishing. The method of claim 5 requires an improvement by an additional deposition process to reshape the filling material deposited on the substrate by the first deposition process, followed by polishing.

Appellants' description of the prior art is in section 2 of the specification on pages 1-5. Appellants admit that the concurrent deposition and etching by bias ECR-CVD to fill grooves and trenches with a filler material is known (page 3, lines 12-17). The concept of "lateral leveling" is also admitted as being well known (page 3, line 20-page 4, line 3). Similarly, it is known that whenever any groove or trench is filled with a filling material, the surface must be smoothed or polished (page 1, line 14-page 2, line 3). Therefore the combination of lateral leveling and polishing is considered to be described in appellants' admitted prior art. As discussed

³ See 37 CFR § 1.75(e)(1993) and *Ex parte Jepson*, 1917 Dec. Comm'r Pats. 62, 243 Off. Gaz. Pat. Off. 525 (1917).

Appeal No. 95-1009
Application 07/858,632

above, the method of claim 1 merely calls for leveling and polishing and these steps are described in the admitted prior art. The method of claim 4 calls for controlling the deposition rate in a manner known as lateral leveling followed by a known polishing step (see the specification, page 15, last paragraph, to page 16, line 19). Thus the admitted prior art is considered to describe the subject matter of claims 1 and 4 within the meaning of § 102(b).

The methods of claims 2 and 5 require an additional deposition of the filling material. This step has not been found to be admittedly known in the prior art as recited on pages 1-5 of the specification. The examiner fails to point out where this step is described in the admitted prior art (see the answer, page 6). Accordingly, the rejection of claims 2 and 5 under 35 U.S.C. § 102(b) in view of the admitted prior art cannot be sustained since every limitation of these claims is not found in the admitted prior art as applied by the examiner. *See In re Bond, supra.*

C. The Rejection in view of Kaanta

The method of claim 6 calls for the improvement in the

process of fabricating electronic devices which include a polishing step which comprises (1) forming a conductive polish-stop layer over a substrate; (2) effecting said smoothing; and (3) monitoring the electric resistance between the substrate and a surface of the polishing member contacting the substrate to determine a polish end according to changes in electric resistance.⁴

Kaanta is directed to a method of monitoring the conductivity of a semiconductor wafer during the course of a polishing process (see the abstract). Kaanta uses an oscilloscope to monitor an electric current (column 4, lines 48-50) which follows a current path when the insulating layer is removed by polishing, exposing the substrate contacting metal pads (column 4, lines 31-39). Therefore Kaanta describes the three steps of the claimed method, i.e., forming a conductive polish-stop layer over a substrate by use of the metal pads⁵ or metal points 4, effecting a smoothing process,

⁴ The lack of an end point detection method in polishing after the ECR-CVD process has been recognized in the prior art (see Wolf, page 239).

⁵ Claim 6 is not limited to a conductive polish-stop layer over the *entire surface* of the substrate. Therefore the formation of metal pads in Kaanta meets the requirement of the first step in the method of claim 6.

and monitoring the electric current (a function of the resistance) between the substrate and a surface of the polishing member to determine a polish end. Appellants argue that Kaanta does not teach monitoring the resistance between the substrate and the surface of a polishing member (main brief, pages 4-5). As noted by the examiner on page 3 of the final rejection, the monitoring of the current (or lack thereof) is a measure of the resistance. In fact, Kaanta teaches that the invention can also be used to directly monitor the resistivity of a conductive layer during the polishing process (column 6, lines 22-24).

Accordingly, we find that Kaanta describes the subject matter of claim 6 within the meaning of 35 U.S.C. § 102(b).

D. The Rejection in view of Olmer

The requirements of claims 1, 2 and 4 have been previously discussed and are incorporated herein.

Olmer discloses a method for depositing a filler material (silicon dioxide) over conductors of an integrated circuit having a high aspect ratio (column 1, lines 8-12).

Simultaneous sputter and deposition occurs which results in uneven net deposition (see column 2, lines 51-55, and Figure 2). To remedy this uneven net deposition (i.e., level it), an additional deposition occurs with subsequent planarization (i.e., smoothing, see column 2, lines 58-64, column 3, lines 50-62, column 5, lines 3-12, and column 5, line 54-column 6, line 14). The uneven initial deposition results in a net thickness of deposition that is lowest at the corners (column 5, lines 6-9, and Figure 2). Therefore Olmer specifically describes leveling the height of portions of the filling material, including leveling achieved by an additional deposition of the filling material, and effecting a deposition process such that the difference in thickness of the filler material between a central portion and a peripheral portion (i.e., the corner) is canceled out (see column 5, lines 9-12).

Olmer discloses a final step of "planarization" which may be accomplished "in a known manner" to yield the smooth surface of Figure 4 (see column 5, lines 62-64). Grinding and etching are taught by Olmer as methods of planarizing the surface (column 5, line 66-column 6, line 5). The polishing step of the method of the appealed claims is not expressly

Appeal No. 95-1009
Application 07/858,632

disclosed. The examiner concludes that "polishing is a form of grinding and/or etching, and would have been an obvious choice for the known manner [of planarizing] of Olmer."

(answer, page 4). Appellants argue that "Olmer fails to teach the techniques of the present invention, whereby the semiconductor substrate is leveled over its entire surface."
(brief, page 3).

However, it is clear that Olmer teaches planarization whereby the semiconductor substrate is leveled over its entire surface (see Figure 4 and column 5, line 62-column 6, line 5). Appellants admit that it is known to accomplish smoothing by using various polishing techniques (specification, page 1). In fact, appellants' definition of "polishing" is broad enough to include the grinding or etching of Olmer (see the specification, pages 1 and 2). Accordingly, it would have been well within the ordinary skill in the art to use polishing to accomplish the planarization of Olmer.

For the foregoing reasons, the rejection of claims 1, 2 and 4 under § 103 as unpatentable over Olmer is affirmed.

E. The New Ground of Rejection

Pursuant to our authority under 37 CFR § 1.196(b), we enter a new ground of rejection of claim 5 under 35 U.S.C. § 103 as unpatentable over Olmer.

The method of claim 5 calls for the reshaping of the filling material by effecting an additional deposition under such conditions that the ratio of deposition rate to etching rate is greater at a peripheral portion than at a central portion of the substrate, with subsequent polishing.

Olmer discloses a reshaping of the filling material by controlling the rate of deposition to the rate of removal so as to give a minimum net deposition at the corners, i.e., more filler is deposited at a peripheral portion than at a central portion. See Olmer, column 2, lines 50-52, 58-60, column 5, lines 6-12, column 6, lines 9-14, and Figures 2 and 3. Olmer teaches that the reshaped surface is subsequently "planarized in a known manner" (column 5, lines 62-64, and Figure 4) such as by etching or grinding (column 5, line 66-column 6, line 5). As previously discussed, the polishing step of appellants' claimed method would have been encompassed by the

Appeal No. 95-1009
Application 07/858,632

steps suggested by Olmer and, regardless, was well known in the prior art.

For the foregoing reasons, we find that the subject matter of claim 5 would have been obvious within the meaning of 35 U.S.C. § 103 in view of Olmer.

F. Summary

The rejection of claims 1 and 3 under 35 U.S.C. § 102(b) in view of Wolf is affirmed. The rejection of claims 1 and 4 under 35 U.S.C. § 102(b) in view of the admitted prior art is affirmed. The rejection of claims 2 and 5 under 35 U.S.C. § 102(b) in view of the admitted prior art is reversed. The rejection of claim 6 under 35 U.S.C. § 102(b) in view of Kaanta is affirmed. The rejection of claims 1, 2 and 4 under 35 U.S.C. § 103 in view of Olmer is affirmed. Pursuant to our authority under 37 CFR § 1.196(b), we enter a new ground of rejection of claim 5 under 35 U.S.C. § 103 as unpatentable over Olmer. Accordingly, the decision of the examiner is affirmed in part.

In addition to affirming the examiner's rejection of one

Appeal No. 95-1009
Application 07/858,632

or more claims, this decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)).

37 CFR § 1.196(b) provides, "A new ground of rejection shall not be considered final for purposes of judicial review."

Regarding any affirmed rejection, 37 CFR § 1.197(b) provides:

(b) Appellant may file a single request for rehearing within two months from the date of the original decision

37 CFR § 1.196(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (37 CFR § 1.197(c)) as to the rejected claims:

(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

(2) Request that the application be reheard

Appeal No. 95-1009
Application 07/858,632

under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

Should the appellant elect to prosecute further before the Primary Examiner pursuant to 37 CFR § 1.196(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before

the examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If the appellant elects prosecution before the examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for reconsideration thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED IN PART - 37 CFR § 1.196(b)

Appeal No. 95-1009
Application 07/858,632

EDWARD C. KIMLIN
Administrative Patent Judge

CHUNG K. PAK
Administrative Patent Judge

THOMAS WALTZ
Administrative Patent Judge

)
)
)
)
) BOARD OF PATENT
) APPEALS AND
) INTERFERENCES
)
)
)

HILL, Van SANTEN, STEADMAN & SIMPSON
70th Floor Sears Tower
Chicago, Illinois 60606

Appeal No. 95-1009
Application 07/858,632

APPENDIX

1. A method of fabricating an electronic device, of the type wherein grooves formed a substrate are filled up with a filling material deposited by a deposition process in which etching and deposition are achieved concurrently, wherein the improvement comprises:

leveling the height of portions of the filling material deposited on these portions of the substrate other than those corresponding to the grooves; and

thereafter, polishing away said portions of the filling material to smooth an entire surface of the substrate.

2. A method according to claim 1, wherein said leveling is achieved by an additional deposition of the filling material.

3. A method according to claim 1, wherein said leveling is achieved by a full surface etch back process.

4. A method of fabricating an electronic device, of the type wherein grooves formed in a substrate are filled up with a filling material deposited by a deposition process in which etching and deposition are achieved concurrently, wherein the improvement comprises:

effecting said deposition process under such conditions that the difference in thickness of the deposited filling material between a central portion and a peripheral portion of the substrate is canceled out; and

thereafter, polishing the substrate to smooth the same.

5. A method of fabricating an electronic device, of the type wherein grooves formed in a substrate are filled up with a filling material deposited by a deposition process in which etching and deposition are achieved concurrently, wherein the improvement comprises:

after said deposition process, effecting an additional deposition process under such conditions that the ratio of deposition rate to etching rate is greater at a peripheral portion than at a central portion of the substrate, thereby reshaping the filling material deposited on the substrate by the first deposition process; and

thereafter, polishing the substrate to smoothen the same.

Appeal No. 95-1009
Application 07/858,632

6. A method of fabricating an electronic device, of the type including a smoothing process achieved by polishing with a polishing member, wherein improvement comprises:

forming a conductive polish-stop layer over a substrate;

effecting said smoothing process; and

during said smoothing process, monitoring the electric resistance between the substrate and a surface of the polishing member contacting the substrate, thereby determining a polish end according to changes in electric resistance.