

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN K. EITRHEIM, RICHARD B. REIS, STEVE MCMAHAN,
LAWRENCE H. HUDEPOHL, DOUGLAS E. DUSCHATKO,
TAI D. NGO and JEFFREY BYRNE

Appeal No. 95-1816
Application 07/859,347¹

ON BRIEF

Before, HAIRSTON, BARRETT and FLEMING **Administrative Patent
Judges.**

FLEMING, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the final rejection of
claims 17 through 24, 26 and 27.

¹Application for patent filed March 27, 1992.

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The invention relates to a low voltage, high frequency electronic processing device.

The independent claim 17 is reproduced as follows:

17. A processor capable of operating at a high clock rate with reduced operating voltage comprising:

- (a) core circuitry that executes instructions;
- (b) bus control circuitry operable to transfer instructions and data between the processor and an external memory;
- (c) memory management circuitry operable to transfer instructions and data between the core circuitry and the external memory;
- (d) clock generation circuitry, coupled to the core circuitry, the memory management circuitry, and the bus control circuitry, for generating at least one clock signal; and
- (e) a plurality of sense amplifiers included in at least one of the core circuitry, the memory management circuitry, the bus control circuitry, and the clock generation circuitry, the plurality of sense amplifiers operable to compress logic thresholds to increase logic switching speed.

The Examiner relies on the following reference:

Ito et al. (Ito) 5,079,745 Jan. 07, 1992

Claims 17 through 24, 26 and 27 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ito.

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Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs² and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 17 through 24, 26 and 27 under 35 U.S.C. § 103.

The Examiner has failed to set forth a **prima facie** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. **In re Sernaker**, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." **Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.**, 73 F.3d 1085, 1087, 37 USPQ2d

²Appellants filed an appeal brief on July 25, 1994. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on October 7, 1994. We will refer to this reply appeal brief as the reply brief. The Examiner responded to the reply brief with a letter, mailed October 18, 1994, stating that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

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1237, 1239 (Fed. Cir. 1995), **cert. denied**, 117 S.Ct. 80 (1996)
citing W. L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d
1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), **cert. denied**, 469
U.S. 851 (1984).

Appellants argue on pages 3 and 4 of the brief that Ito fails to teach or suggest a processor comprising core circuitry that executes instructions, bus control circuitry, memory management circuit operable to transfer instructions and data between the core circuitry and memory, clock generation circuitry and a plurality of sense amplifiers in at least one of the core circuitry, the memory management circuitry, the bus control circuitry and clock generation circuitry such that the plurality of sense amplifiers are operable to compress logic thresholds to increase logic switching speed as recited in Appellants' claims. Appellants further emphasize on page 2 of the reply brief that Ito fails to teach or suggest a processor using sense amplifiers to allow the processor to operate at a high clock rate with reduced voltages as recited in Appellants' claims.

Ito teaches a memory using sense amplifiers. However, Ito fails to teach a processor capable of operating at a high clock

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rate with reduced operating voltages comprising core circuitry that executes instructions, bus control circuitry, memory management circuit operable to transfer instructions and data between the core circuitry and memory, clock generation circuitry and a plurality of sense amplifiers in at least one of the core circuitry, the memory management circuitry, the bus control circuitry and clock generation circuitry such that the plurality of sense amplifiers are operable to compress logic thresholds to increase logic switching speed as recited in Appellants' claims. Ito teaches in column 1, lines 5-10, that the field of the invention relates to a sense amplifier in a semiconductor memory. Ito teaches in columns 4 and 5 a memory having a sense amplifier connected to first and second bit lines for amplifying the potential difference. Furthermore, we note that Ito only claims in columns 6 through 8 a sense amplifier for amplifying a signal stored in a memory cell for reading and a memory comprising a sense amplifier connected to first and second bit lines of the memory for amplifying the potential difference. Therefore, we fail to find that Ito teaches a processor or a processor device as recited in Appellants' claims.

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Furthermore, we fail to find any suggestion of modifying Ito memory to provide a processor comprising core circuitry that executes instructions, bus control circuitry, memory management circuit operable to transfer instructions and data between the core circuitry and memory, clock generation circuitry and a plurality of sense amplifiers in at least one of the core circuitry, the memory management circuitry, the bus control circuitry and clock generation circuitry such that the plurality of sense amplifiers are operable to compress logic thresholds to increase logic switching speed as recited in Appellants' claims. The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg.***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

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We have not sustained the rejection of claims 17 through 24, 26 and 27 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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MICHAEL R. FLEMING)	
Administrative Patent Judge)	

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Cyrix Corporation
P.O. Box 853919
MS 250
Richardson, TX 75085-3919