

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PHILLIP E. MATTISON

Appeal No. 95-1851
Application 07/902,186¹

ON BRIEF

Before HAIRSTON, JERRY SMITH and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-4.² We reverse.

¹ Application filed June 22, 1992.

² Appellant's Amendment C (Paper No. 7) is indicated on the file wrapper as not having been entered. However, the appeal brief at 1 states that the examiner indicated that the amendment would be entered upon the filing of an appeal and assumes that the amendment will be entered. The examiner's answer states on page 1 that "appellant's statement of the status of amendments after final rejection contained in the brief is correct." The examiner's answer also states that the statement of the status of

said frame buffer memory means to said display means;

frame buffer write detect means for detecting a write of a new value of display data into said frame buffer memory means;

address detect means coupled to said frame buffer write detect means for determining an affected address where said new value of display data is stored within said frame buffer memory means in response to said frame buffer write detect means;

address translate logic means for generating an appropriate start address for updating said display means based on said affected address within said frame buffer memory means where said new value of display data was stored; and

blocking means for selectively blocking memory accesses to said frame buffer memory means which fall outside the range of applicable display data for said display means.

3. A method for providing automatic virtual display panning for driving VGA display data on a lower resolution display consisting of the steps of:

providing frame buffer memory means for storing a full resolution VGA image;

providing display means coupled to said frame buffer memory means and having a resolution less than the resolution of said frame buffer memory means for providing a display;

providing VGA controller means for transferring display data in said frame buffer memory means to said display means;

providing frame buffer write detect means for detecting a write of a new value of display data into said frame buffer memory means;

providing address detect means coupled to said frame buffer write detect means for determining an affected

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address where said new value of display data is stored within said frame buffer memory means in response to said frame buffer write detect means;

providing address translate logic means for generating an appropriate start address for updating said display means based on said affected address within said frame buffer memory means where said new value of display data was stored; and

providing blocking means for selectively blocking memory accesses to said frame buffer memory means which fall outside the range of applicable display data for said display means.

Opinion

On pages 2-3 of the answer, the examiner specifically describes the teachings of Belch. Notably absent from that description is any discussion of displaying full resolution VGA display data on a "lower" resolution display device. Of course, there is no discussion about any address translation to produce a starting address for updating the "lower" resolution display device. The examiner has pointed to nothing in Belch which discusses the use of a "lower" resolution display device.

Nonetheless, the examiner concludes on page 3 of the answer: "It would have been obvious to have a lower resolution display in Belch's circuit for displaying high resolution data since Belch's display can present only a part of the data stored in a memory(IS) (see column 1, lines 11-13)." The examiner further states on the same page: "The use of a VGA controller as a

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display controller would have been an obvious expedient as it is a standard in the art to provide a VGA resolution since it is well-known in a display system for providing a high quality color display to a user (for example, see the discussion by Berry)."

The examiner's obviousness conclusion is without merit and his rationale is misplaced.

The appellant is not claiming simply a VGA controller for displaying VGA resolution display data. Rather, the invention's apparent novelty is directed to the selection of a portion of high resolution VGA display data based on addressed display data and to display the selected portion on a display device of "lower" resolution.

Independent apparatus claim 1 requires a frame buffer memory means for storing a full resolution VGA image, a display means having a resolution "less" than the resolution of the frame buffer memory means for providing a display, and VGA controller means for transferring display data in the frame buffer memory means to the lower resolution display means. Claim 1 further recites an address translate logic means for generating an appropriate start address for updating the display means. Corresponding steps are recited in independent process claim 3. The claimed invention requires actual display of selected data on

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a "lower" resolution display.

It is true that Belch discloses a display system which contains more image information in memory than may be displayed all at one time. But it does not reasonably suggest address translation to produce a starting address for updating a display means of lower resolution. The examiner has pointed to nothing in Belch which suggests displaying data on a display device of a different resolution than that originally intended and with respect to which the full resolution VGA image is compatible. We do not see how the fact that more data is stored than that which can be together displayed on a lower resolution display would have reasonably suggested displaying selected data on a "lower" resolution display device.

While displaying data on a lower resolution device results in not having the entire image being displayed at the same time, it does not follow that if the entire image is not being displayed at the same time then a display device of lower resolution must have been or is being used. Belch teaches how to display a variable mosaic of plural images which together are too large to be displayed all at once, without need to shift or move data around each time the mosaic is changed. We do not find Belch as reasonably providing the necessary motivation or

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reasonable suggestion to one with ordinary skill in the art to display a selected portion of high resolution data on a display device of "lower" resolution. Displaying only a part of the stored image data is readily achievable by use of the same display device.

The examiner evidently regards any display device which does not display the entirety of the image stored in memory as a "lower resolution display device" (Paper No. 14, lines 3-10). As the appellant points out (Supp. Reply. at 2), that is incorrect. The examiner's position is clearly erroneous in that regard. The appellant correctly states that the terms high and low resolution monitors or display devices do not depend on whether or not the display system can display all of the display data stored in memory. Rather, the terms are based on the size of the display system's pixel matrix. The appellant's specification does not define a different meaning for high and low resolution display than that commonly recognized in the art. Indeed, the specification discusses display resolution by reference to the size of the pixel matrix (see Summary of Invention and also page 5 of the specification).

Claim 2 depends from claim 1 and thus includes all limitations of claim 1. Claim 4 depends from claim 3 and thus

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includes all limitations of claim 3. If the rejection of claims 1 and 3 cannot be sustained, the rejection of claims 2 and 4 also cannot be sustained.

For the foregoing reasons, we do not sustain the rejection of claims 1-4 under 35 U.S.C. § 103 as being unpatentable over Belch.

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Conclusion

The rejection of claims 1-4 under 35 U.S.C. § 103 as being unpatentable over Belch is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
JERRY SMITH)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
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