THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte SATWINDER MALHI

Appeal No. 95-1898
Application 07/883,985[1]

ON BRIEF

Before THOMAS, HAIRSTON, and JERRY SMITH, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed May 18, 1992.

This is an appeal from the final rejection of claims 1 and 5 through 10. Claims 2 through 4 and 11 through 13 have been canceled.

The disclosed invention relates to a high voltage power transistor in which the source and the drain are both formed at a top surface of the transistor, and the gate is formed in a trench between the source and the drain. A dielectric lining is located in the trench to separate the gate from both the source and the drain. A relatively thin portion of the dielectric is located adjacent to the source, and a relatively thick portion of the dielectric is located adjacent to the drain.

Claims 1 and 6 are illustrative of the claimed invention, and they read as follows:

1. A high voltage power transistor, comprising:

a source formed at a top surface of the transistor;

a drain formed at the top surface of the transistor;

a gate formed in a trench between the source and drain; and

a nonuniform dielectric lining in the trench having a thin portion adjacent the source and a thick portion adjacent the drain.

6. A high voltage power transistor, comprising:

a substrate;

a drift region formed in a top face of the substrate;

a drain region formed in the drift region;

a p-well region formed in the top face of the substrate;

a source region formed in the p-well region;

a trench formed in the top face of the substrate between the drift region and the p-well region such that the trench makes contact with both the drift region and the p-well region;

a nonuniform dielectric lining in the trench having a thin portion adjacent the p-well region and a thick portion adjacent the drift region; and

a gate formed within the trench.

The references relied on by the examiner are:

Blanchard	4,914,058	Apr. 3, 1990
Contiero et al. (Contiero)	4,949,142	Aug. 14, 1990

Claims 1 and 5 through 10 stand rejected under 35 U.S.C. § 103 as being unpatentable over Blanchard in view of Contiero.

Reference is made to the brief and the answer for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 103 rejection of claims 1 and 5 through 10.

According to the examiner (Answer, page 3), Figure 3 of the reference to Blanchard discloses a power MOS transistor that comprises a source 21a, a drain region 10, a gate formed in a trench between the source and the drain, and a nonuniform oxide dielectric lining 32 in the trench that has a thin portion adjacent the source, and a thick portion adjacent the drain. The examiner makes clear in the response (Answer, page 4) to appellant's arguments that the drain regions 10 and 11 in Blanchard are located in the bottom surface of the transistor. The examiner states (Answer, page 3) that Figure 2 of the reference to Contiero discloses "a power MOS transistor in which a source and a drain are formed to either side of a gate and at a top surface of a substrate." The reference to Contiero does indeed disclose such structure, but the gate is not formed in a trench between the source and the gate. As seen in Figure 2 of

Contiero, the gate electrodes 131 through 144 are formed on the top surface of the transistor, and each gate electrode is surrounded by dielectric insulation. From these teachings, the examiner concludes (Answer, page 4) that:

> [T]o provide the device of Blanchard with a drain at a top surface of a substrate as taught by Contiero et al. would have been obvious to one of ordinary skill in this art because Contiero et al. teach the same type device as Blanchard with the same purpose, however Contiero et al. teach an effective manner of forming the drain at the top surface of the device.

In the response to appellant's arguments (Answer, pages 4 and 5), the examiner further explains that: Blanchard discloses a lightly doped (N) drain region 11 with a bottom heavily doped (N+) drain contact region 10; and Contiero teaches that it is advantageous to integrate vertical power DMOS devices of the type having a lightly doped (N) drain region 116 at a top surface of the transistor, and a buried heavily doped (N+) drain contact region 112 by forming the devices on a P substrate, and by bringing up a N+ heavily doped contact region 112a to the top surface to form a contact away from the area of the actual device.

Notwithstanding the fact that "Contiero et al. teach the same

type device as Blanchard with the same purpose," and that both devices teach a lightly doped drain region and a highly doped drain region, we are still not convinced by evidence of record, and the reasoning advanced by the examiner, that the skilled artisan would have known after reviewing the teachings and suggestions of Contiero to undertake a wholesale redesign of the drain structure of Blanchard to meet the limitations of appellant's claimed power transistor. Even if we assume for the sake of argument that the skilled artisan would have known to bring the buried heavily doped drain region in Blanchard to the top surface of the transistor via a sinker region, we are still left with the unsolved question of where the sinker region extension from the buried heavily doped drain region would break the surface of the transistor. The Examiner's Answer certainly does not shed any light on this question. If the drain extension breaks the surface of the transistor adjacent the source regions 21a and 21b in Blanchard, then the claim language "a gate formed in a trench between the source and drain" certainly will not be met by the modified transistor of Blanchard. Another unsolved

question is what type of transistor will be created by such a drain extension to the surface of the transistor in Blanchard. The Examiner's Answer is silent on this point. In view of these unanswered questions, it appears to us that the examiner is impermissibly using the claims as a road map to piece together a rejection from wholly different power transistor teachings. Inasmuch as we are uncertain as to where this rejection is taking us, we will reverse the 35 U.S.C. § 103 rejection of claims 1 and 5 through 10.

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DECISION

The decision of the examiner rejecting claims 1 and 5 through 10 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)
Administrative Patent Judge)
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) BOARD OF PATENT
KENNETH W. HAIRSTON)
Administrative Patent Judge) APPEALS AND
)
) INTERFERENCES
JERRY SMITH)
Administrative Patent Judge)

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Robby T. Holland
TEXAS INSTRUMENTS INCORPORATED
P.O. Box 655474 - M/S 219
Dallas, TX 75265