

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

This opinion (1) was not written for publication and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEFAN BLIXT

Appeal No. 95-2572
Application 08/157,451

ON BRIEF

Before JERRY SMITH, TORCZON, and CARMICHAEL, Administrative Patent Judges.

TORCZON, Administrative Patent Judge.

OPINION

We have reviewed the record in its entirety in light of the arguments of Appellant and the examiner. Our decision presumes familiarity with the entire record. A preponderance of the evidence of record supports each of the following fact findings.

A. The nature of the case

This is an appeal under 35 U.S.C. § 134 from the final rejection of claims 10-15. (Paper 24 (Not. App.)). No other claims are pending. (Paper 23 at 1.) We reverse.

Appellant filed the subject application on 17 December 1990. He claims the priority of United States patent application

07/627,864, filed 17 December 1990 (now abandoned), under 35 U.S.C. § 120. He also claims the priority of Swedish patent application 9000083-7, filed 10 January 1990, under 35 U.S.C. § 119. (Paper 19 (Req. Appl'n under 1.62) at 2.)

The subject matter of the invention relates to a graphics processor for raster displays. (Paper 1 at 1.) Claim 15, the only independent claim, defines the subject matter as follows (Paper 22 (Amdt. entered 11 May 1994) at 1-2, enumeration from Fig. 2¹):

A graphics processor **16** for writing information representing at least a part of an image into an image buffer **18** of predetermined size, comprising:

- (a) high level graphics processor means **30** for converting high level graphics instructions into low level graphics instructions, at least some of which contain pixel data;
- (b) queue memory means **34** connected to said high level graphics processor means **30**, for receiving and storing said low level graphics instructions in the order they are generated by said high level graphics processor means **30**; and
- (c) low level graphics processor means **32** connected to said queue memory means **34** and said image buffer **18**, for reading and executing said low level graphics instructions from said queue memory means **34** one after the other and for repeatedly copying at least some of said pixel data into different memory locations of said image

¹ Figure 1 should be labeled "Prior Art" for clarity. Manual of Patent Examining Procedure (MPEP) § 608.02(g).

buffer **18** corresponding to different positions in said image as specified by said low level graphics instructions.

B. The rejection

The examiner relied on the following references in rejecting the claims:

J.M. Rosenberg, Dictionary of Computers, Information Processing, and Telecommunications 358-59, 384-86 (2d ed. 1987).

Feldman et al. (Feldman)	4,769,715	6 Sep. 1988
Dalrymple et al. (Dalrymple)	4,862,155	29 Aug. 1989
Hannah	4,991,110	5 Feb. 1991 (filed 13 Sep. 1988)
Ebbers et al. (Ebbers)	5,001,672	19 Mar. 1991 (filed 16 May 1989)

Specifically, the examiner rejected claim 15 under 35 U.S.C. § 103 as obvious in view of Dalrymple and Feldman. (Paper 23 at 2.) Claim 15 is the only independent claim on appeal and Appellant states that the claims stand or fall together (Paper 25 (App. Br.) at 3), so we will not consider the remaining rejections separately. In re Geisler, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1367 (Fed. Cir. 1997)

Dalrymple discloses a graphics display system in which a control processor stores primary display lists in memory. A picture processor processes the primary display lists to provide control data and pixel data to an image buffer in a display controller. (2:35-54.) Contrary to the examiner's position, we

find that the claimed high-level graphics processor means corresponds to the picture processor, which converts high-level display lists into control and pixel data suitable for use by the display controller. The control processor may further process to control and pixel data to produce a secondary pixel image and incorporate this image into a secondary display list. (2:55-3:5.) This secondary display list may then be sent to the picture processor for further minimal processing before it is sent to the display controller. (3:6-24.) It might be possible to construe the control processor and routing circuit as the low-level graphics processor means. However, it is not clear to us on the record developed thus far that our reading of Dalrymple would provide a basis for entering a new ground of rejection based on our construction.

The examiner relies on Feldman for the teaching of run-length encoding. Although we agree with the examiner that run-length encoding is relevant to the problem facing the inventor, Feldman does not cure the deficiencies in the examiner's reading of Dalrymple. The record does not suggest, and we do not find, that any combination of the other references cures the deficiencies in the examiner's reading of Dalrymple.

The combination of Dalrymple and Feldman would not have rendered claim 15 obvious for the reasons the examiner proposes. The remaining claims depend from claim 15 and their rejections

depend on the examiner's erroneous reading of Dalrymple. Thus, they would not have been rendered obvious for the reasons the examiner urges.

DECISION

We reverse the rejection of claims 10-15 under section 103.

REVERSED

JERRY SMITH)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
RICHARD TORCZON)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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