

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

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Paper No.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RALPH G. WHITTEN, RICHARD L. BECHTEL,
MAMMEN THOMAS, HUA-THYE CHUA, ANDREW K. CHAN,
and JOHN M. BIRKNER

Appeal No. 95-2914
Application No. 07/447,969¹

HEARD: Apr. 9, 1999

Before JOHN D. SMITH, PAK, and KRATZ, Administrative Patent Judges.

KRATZ, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1-6, 9, 10, 28-34, 36, and 39, which are all of the claims pending in this application.

¹ Application for patent filed December 8, 1989. According to appellants, this application is a continuation-in-part of Application 07/404,996, filed September 7, 1989.

BACKGROUND

The appellants' invention relates to a method for fabricating a programmable interconnect structure having a low leakage current in the preprogrammed state of less than 10 nanoamperes at 5.5 volts via plasma enhanced chemical vapor deposited amorphous silicon features located between and contacting two separate conductors. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A method for fabricating a programmable interconnect structure for an integrated circuit, comprising the steps of:

fabricating a first conductor;

fabricating an insulating layer overlaying said first conductor;

fabricating an opening through said insulating layer at a selected location and terminating said opening at a portion of said first conductor;

depositing using plasma enhanced chemical vapor deposition a film of amorphous silicon upon said insulating layer and in said opening;

patterning said amorphous silicon film to form in said opening at said selected location an amorphous silicon feature, said feature contacting and fully overlaying said first conductor portion; and

fabricating a second conductor, wherein a portion of said second conductor contacts and overlays said amorphous silicon feature;

wherein the process parameters of said plasma enhanced chemical vapor deposition include a temperature and gaseous environment selected to yield a leakage current at said location of less than about 10 nanoamperes at 5.5 volts.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

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| Ovshinsky et al. (Ovshinsky I) 1980 | 4,217,374 | Aug. 12, |
| Ovshinsky et al. (Ovshinsky II) 1980 | 4,226,898 | Oct. 07, |
| Holmberg et al. (Holmberg I) 12, 1985 | 4,499,557 | Feb. |
| Holmberg et al. (Holmberg II) 08, 1986 | 4,599,705 | July |
| Kanai et al. (Kanai) 1988 | 4,771,015 | Sep. 13, |

Cook et al., Amorphous Silicon Antifuse Technology For Bipolar Proms, IEEE Bipolar Circuits and Technology Meeting, 1986, pp. 99 and 100, (Cook).

Claims 1-6, 28, and 32-34 stand rejected under 35 U.S.C. § 103 as being unpatentable over Holmberg I or II each in view of any of Ovshinsky I, Ovshinsky II, or Kanai.

Claims 9, 10, 29-31, 36 and 39 are rejected under 35 U.S.C. § 103 as being unpatentable over Holmberg I or II each in view of any of Ovshinsky I, Ovshinsky II, or Kanai as applied to claims 1-6, 28, and 32-34 above, and further in view of Cook.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellant and the examiner in the respective briefs and answers thereto. In so doing, we find ourselves in agreement with appellants' basic contention that the examiner has not carried his burden of establishing a *prima facie* case of obviousness of the claimed subject matter. Accordingly, we will not sustain the examiner's rejections.

The examiner acknowledges that neither Holmberg reference teaches the selection of the process parameters of the plasma enhanced chemical vapor deposition of an amorphous silica film including the temperature and gaseous environment thereof so

as to obtain a leakage current of less than about 10 nanoamperes at 5.5 volts at the amorphous silicon feature as required by all of the appealed claims (answer, page 4). According to the examiner, a skilled artisan would inherently or obviously have arrived at the claimed leakage value and depositing conditions by using the deposition parameters and conditions of any of Ovshinsky I, Ovshinsky II, or Kanai for preparing the amorphous silicon feature in the process of either Holmberg patent (answer, page 5). However, the examiner has not furnished an adequate basis in fact and/or technical reasoning to reasonably support the conclusion that the claimed current leakage would have necessarily flowed from the combined teachings of the applied prior art references. See Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Int. 1990). In this regard, we note that the examiner has not satisfactorily explained how the teaching of an off resistance of 10,000 to 1,000,000 ohms for the cell in either Holmberg I or II (column 4, of each) would have necessarily or obviously suggested a current leakage for the amorphous silicon feature as low as provided for in the appealed claims based on the present record. Moreover, as

noted by appellants (brief, page 13), Holmberg I suggests lowering the resistivity of the amorphous silicon via doping rather than furnishing any suggestion of using a method of raising the resistivity to levels sufficient to obtain the claimed low leakage current method of fabrication.

Furthermore, we agree with appellants that the examiner has not adequately explained how the deficiency of the primary references is overcome by the applied alternative secondary references.

In our view, the examiner has not satisfactorily explained how the combined teachings of the applied Holmberg I or II taken with any of Ovshinsky I or II, or Kanai would have suggested or led a skilled artisan to arrive at the process required by all of the appealed claims including the step of plasma enhanced chemical vapor depositing an amorphous silicon film under conditions selected to yield an interconnect structure with a leakage current below 10 nanoamperes at 5.5 volts at the location of the amorphous silicon deposit. The Cook reference as additionally applied to claims 9, 10, 29-31, 36 and 39 does not cure this deficiency. Having carefully considered all of the arguments advanced by appellants and the

examiner, we find ourselves in agreement with appellants that the aforementioned rejections are not well founded. Accordingly, these rejections will be reversed. In view of the above, we find it unnecessary to reach or discuss the rebuttal evidence furnished by appellants.

CONCLUSION

To summarize, the decision of the examiner to reject claims claims 1-6, 28, and 32-34 under 35 U.S.C. § 103 as being unpatentable over Holmberg I or II each in view of any of Ovshinsky I, Ovshinsky II, or Kanai; and to reject claims 9, 10, 29-31, 36 and 39 under 35 U.S.C. § 103 as being unpatentable over Holmberg I or II each in view of any of Ovshinsky I, Ovshinsky II, or Kanai as above further in view of Cook is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED

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| JOHN D. SMITH |) | |
| Administrative Patent Judge |) | |
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| |) | BOARD OF PATENT |
| CHUNG K. PAK |) | APPEALS |
| Administrative Patent Judge |) | AND |
| |) | INTERFERENCES |
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| PETER F. KRATZ |) | |
| Administrative Patent Judge |) | |

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David H. Carroll
Skjerven, Morrill, MacPherson,
Franklin & Friel
25 Metro Drive, Suite 700
San Jose, CA 95110

APPEAL NO. - JUDGE KRATZ
APPLICATION NO. 07/447,969

APJ KRATZ

APJ JOHN D. SMITH

APJ PAK

DECISION: **REVERSED**

Prepared By: TINA

DRAFT TYPED: 12 Jan 00

FINAL TYPED: