

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FUK HO P. NG
and SHIVALING S. MAHANT-SHETTI

Appeal No. 95-3193
Application 07/954,133¹

ON BRIEF

Before THOMAS, JERRY SMITH and CARMICHAEL, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-57. Amendments

¹ Application for patent filed September 30, 1992.

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after final rejection were filed on June 6, 1994 and September 1, 1994, and both amendments were entered by the examiner. The first amendment cancelled claims 17-29 and 45-57 from the application. The cancellation of these claims rendered moot the final rejection of these claims under 35 U.S.C. § 101. Therefore, only claims 1-16 and 30-44 are now on appeal before us.

The invention pertains to an apparatus for subtracting or adding two thermometer coded words which each include a plurality of bytes. In thermometer coding, the value of a number is represented by a number of right justified "1" bits. For example, the number "3" would be represented as 0111 in a four bit system. Obviously, as the number to be represented increases, the number of bits required to represent the number grows rapidly. One way to reduce the amount of circuitry necessary to operate on thermometer coded numbers is to code each digit or byte of a number as a separate thermometer coded value. For example, in the same four bit system, the number "31" would be represented as 0111 0001 with each digit coded separately.

Representative claim 1 is reproduced as follows:

1. A device for subtracting two thermometer coded words which each include a plurality of bytes, comprising:
circuitry for determining a presence of a first relationship between said words;

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circuitry for determining a presence of a second relationship between said words;

circuitry for decreasing a value of a first most significant byte corresponding to a first said word in response to said presence of said first relationship;

circuitry for decreasing a value of a second most significant byte corresponding to a second said word in response to said second relationship;

circuitry for subtracting the value of said first most significant byte from the value of said second most significant byte to obtain a first result; and

circuitry for reconstructing said first result into proper thermometer code format.

No references are relied on by the examiner.

Claims 1-16 and 30-44 only stand rejected under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the invention.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner, and the arguments set forth by the examiner in support of the rejection for indefiniteness. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set

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forth in the briefs in support of their position that the claims are in compliance with the second paragraph of 35 U.S.C. § 112..

It is our view, after consideration of the record before us, that claims 1-16 and 30-44 particularly point out the invention in a manner which complies with 35 U.S.C. § 112. Accordingly, we reverse.

Appellants nominally indicate in their brief that all the claims stand or fall together for purposes of this appeal [brief, page 3]. The examiner's rejection, however, points to the alleged indefiniteness of certain specific claims, and appellants' arguments address these claims separately in the arguments portion of the brief. Therefore, we will consider separately those claims separately argued by appellants to the extent necessary to properly dispose of this appeal. All claims not specifically argued will stand or fall with the claims from which they respectively depend. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

With respect to claim 1, the examiner asserts that the "circuitry for subtracting" in lines 10-11 is indefinite because (1) it is unclear whether the initial or modified values are

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involved in the subtracting, and (2) the claim language does not require the first most significant byte to be smaller than the value of the second most significant byte [answer, pages 2-3]. Appellants argue that claim 1 is definite and that the examiner is unnecessarily requiring them to limit the claim under the rubric of indefiniteness [brief, page 4 and reply brief, page 2]. We conclude that the examiner has erred in determining that claim 1 is not in compliance with 35 U.S.C. § 112.

The general rule is that a claim must set out and circumscribe a particular area with a reasonable degree of precision and particularity when read in light of the disclosure as it would be by the artisan. In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971). Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed in light of the specification. Seattle Box Co., v. Industrial Crating & Packing, Inc., 731 F.2d 818, 826, 221 USPQ 568, 574 (Fed. Cir. 1984). Finally, the legal standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope. In re Warmerdam, 33 F.3d 1354, 1361, 31 USPQ2d 1754, 1759 (Fed. Cir. 1994).

Considering the first point raised by the examiner above, we are of the view that the examiner has confused the contingent

functional operation of the invention with indefiniteness of the structure. The circuitry recited in claim 1 is basically shown in FIG. 1 of the drawings. The claimed circuitry for subtracting is represented by block 24 which receives inputs from blocks 16 and 22. Blocks 16 and 22 respectively receive the most significant bytes of the first and second words. Blocks 16 and 22 either pass the most significant byte unchanged or decrease one of the bytes depending on whether certain conditions are satisfied. The fact that the subtractor may receive different values based on the conditions claimed does not render the connection between the subtractor and the blocks 16 and 22 indefinite. In other words, a subtractor connected to two registers would not be deemed indefinite simply because the values stored in the registers are subject to change. The artisan would have recognized that the claimed subtracting circuitry operates on the original values or the decreased values of the most significant bytes depending on whether or not the claimed conditions have been satisfied. Thus, we find nothing indefinite about the connection of the circuitry for subtracting as recited in claim 1.

Considering the second point raised by the examiner above, we are of the view that the examiner has misunderstood the invention. The examiner's assertion that the smaller value must

be subtracted from the larger value appears contrary to the disclosed invention. The subtractor 24 is described as being an absolute value subtractor which performs the subtraction by performing an exclusive-OR operation on each of the bits of the most significant byte of each word. Thus, the invention as disclosed performs the subtraction without regard to which of the two values is the larger. In other words, the "condition" required by the examiner that the claim be limited to the smaller value being subtracted from the larger value is without support in the description of the invention.

With respect to claim 2, the examiner asserts that the claim is indefinite as to which byte is subtracted from which byte [answer, page 3]. This alleged indefiniteness is in error for the same reasons we just discussed. The least significant byte subtractor of the invention is an absolute value exclusive-OR type subtractor just as the most significant byte subtractor is [see FIG. 6]. Again, the subtraction is not performed in any order as the absolute value is determined.

Also with respect to claim 2, the examiner asserts that the "circuitry for subtracting" must be capable of subtracting a translated byte from an untranslated byte and an untranslated byte from a translated byte, but the recited circuitry is only capable of doing one of these subtractions. We do not agree. The subtractor 32 is connected to translators 28 and 30, and it

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receives a translated value or an untranslated value from each translator depending upon whether or not the claimed conditions are satisfied. Since the subtractors of the invention are not ordered as discussed above, the subtractor as recited in claim 2 correctly describes the invention which allows for either the first word or the second word to be modified or not modified and an absolute value of the difference to be determined.

With respect to claim 30, the examiner asserts that the "reversing circuitry" is not clearly related to the other recited elements [answer, page 4]. The examiner indicates that the claim language does not clearly call for the reverse order byte to be involved in the addition. Again, we do not agree. The adding circuitry clearly operates on a first least significant byte and a second least significant byte, and the reversing circuitry clearly reverses one of these bytes with respect to the other. These two bytes are only identified as the inputs to the adder. That is where the reversing would take place. We also observe that since the claim is directed to a combination of apparatus, it does not matter whether the reversing circuitry is claimed before or after the adding circuitry. The manner in which the reversing circuitry interconnects with the other components would be clear to the artisan.

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Also with respect to claim 30, the examiner asserts that the "circuitry for reconstructing" as recited in the claim is not capable of performing both functions to obtain the required reconstructed first result. Claim 30 recites that a first result or an inverted first result is obtained based on the condition of a first carry. The circuitry for reconstructing is clearly connected to whatever result is obtained, either unchanged or inverted. Thus, the reconstructing circuitry is capable of performing both functions because it receives as input whichever result the recited condition warrants [see FIG. 8].

In conclusion, we find each of the examiner's assertions of indefiniteness to be based upon an improper reading of the claims or of the disclosed invention. We agree with appellants that the artisan having considered the specification of this application would have no difficulty ascertaining the scope of the invention recited in claims 1-16 and 30-44. Therefore, the rejection of these claims under the second paragraph of 35 U.S.C. § 112 is not sustained.

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