

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte BRIAN K. HERBERT

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Appeal No. 95-4815  
Application 08/065,387<sup>1</sup>

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ON BRIEF

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Before THOMAS, KRASS, and TORCZON, Administrative Patent  
Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of  
claims 1 through 9, all of the claims pending in the  
application.

The invention pertains to step addressing in a video RAM.  
More particularly, data words intended for consecutive address  
locations are intercepted and distributed into video RAM at  
evenly spaced, non-consecutive addresses so that when a

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<sup>1</sup> Application for patent filed May 20, 1993.

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graphics controller generates pixels on a display, based on these evenly spaced addresses, the pixels will automatically occupy a vertical column on the display. Thus, the invention permits CPU addressing of data in rows (consecutively) and subsequent writing to video RAM in columns (non-consecutively) with an intermediate graphics controller performing the translation from consecutive to non-consecutive addresses, which saves CPU processing time.

Representative independent claim 1 is reproduced as follows:

1. A method of copying data to video RAM in a computer, comprising the following steps:
  - (a) ordering a processor to copy a consecutive data field to consecutive addresses in video RAM; and
  - (b) receiving the consecutive data field from the processor, and distributing it to non-consecutive addresses in video RAM.

The examiner relies on the following references:

Maruko	4,613,852	Sep. 23, 1986
Diepstraten et al. (Diepstraten)	5,231,383	Jul. 27, 1993 (filed Mar. 25, 1991)

Claims 1 through 9 stand rejected under 35 U.S.C. ' 103. As evidence of obviousness, the examiner cites Diepstraten with regard to claims 1 through 3, 8 and 9, adding Maruko with regard to claims 4 through 7.

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Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

We will sustain the rejection of claims 2 and 8 under 35 U.S.C. ' 103 but we will not sustain the rejection of claims 1, 3 through 7 and 9 under 35 U.S.C. ' 103.

With regard to independent claim 1, the claim calls for a two-step method of copying data to a video RAM. First, a processor is ordered to copy a consecutive data field to consecutive addresses in a video RAM. Clearly, this is part of the prior art and is fairly suggested by Diepstraten.

The second step requires receiving the consecutive data field from the processor and distributing it to non-consecutive addresses in video RAM. Apparently, there is no dispute that Diepstraten does disclose non-consecutive addressing in video RAM. See, for example, appellant's statements, at page 7 of the brief, that "any non-consecutive addressing for data in area 60 is accomplished by the processor itself" and "...the data may be distributed in non-consecutive addresses in RAM."

The key issue, as we view it, is the claim requirement of "receiving the consecutive data field from the processor."

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This means that something must receive the output from the processor and that that output must be the "consecutive data field," as claimed. That something, as disclosed by appellant, is an interface between the processor and the video RAM as shown, for example, in instant Figure 9.

While the examiner is correct in asserting that Diepstraten does discuss the use of contiguous addresses in the video RAM at column 1, lines 41-61, there is no indication therein that anything receives a consecutive data field from the processor. If, in fact, the VRAM control 26 of Diepstraten, as shown in Figure 1 of the patent and, in more detail, in Figure 4, accepted a consecutive data field from graphics processor 22 and then distributed this consecutive data field to non-consecutive addresses in VRAM 30, then we would agree that the rejection under 35 U.S.C. ' 103 would have been proper. However, we find no indication in Diepstraten, and the examiner has not pointed to anything therein to convince us, that VRAM control 26 does, in fact, accept a consecutive data field from processor 22 and distribute it to non-consecutive addresses in VRAM 30. In fact, it would appear that Diepstraten operates as contended by appellant, at page 7 of the brief. That is,

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Any type of non-consecutive addressing for memory region 60 [of VRAM 30] must be performed by the processor itself. Hence, although the data may be distributed in non-consecutive addresses in RAM, it was initially generated by the processor as non-consecutively addressed data.

The examiner has pointed to nothing within the disclosure of Diepstraten that would contradict this reading of the reference. Clearly, if the non-consecutive addressing was already performed by the processor, there would be nothing to receive "the consecutive data field from the processor," as claimed.

Accordingly, we will not sustain the rejection of claim 1 under 35 U.S.C. ' 103.

However, when we consider claim 2, we reach an opposite result. This claim does not require anything to receive a consecutive data field from the processor. The graphics processor 22, itself, in Diepstraten, may be both the means for receiving a stream of data words with associated consecutive addresses and the means for distributing that stream of data words into VRAM at non-consecutive addresses. With regard to the claim limitation of "evenly spaced addresses," we agree with the examiner's reasoning, at page 5 of the answer, that Figure 2 of the reference clearly shows the rows of region 60 within Diepstraten's VRAM being evenly

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spaced in that there are 385 addresses between the first and second rows and there are also 385 addresses between the second and third rows.

Therefore, we will sustain the rejection of claim 2 under 35 U.S.C. ' 103.

With regard to claim 3, this claim contains the requirement, as does claim 1, that something actually receives the consecutive data field from the processor and distribute it to non-consecutive addresses (in the case of claim 3, those non-consecutive addresses are also evenly spaced). Therefore, for the reasons supra, we will not sustain the rejection of claim 3 under 35 U.S.C. ' 103.

With regard to claims 4 through 7, we will not sustain the rejection under 35 U.S.C. ' 103 because the claims all contain the limitation that the writing of character data into video RAM be done "within 80 clock cycles..."

The examiner recognized that Diepstraten disclosed nothing regarding the speed at which writing character data into VRAM was performed but the examiner relied on Maruko for the teaching of providing character data to a display memory in the form of an 8 x 10 array of pixels. The examiner then concluded that it would have been obvious to use the character

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data described by Maruko in the display system of Diepstraten and that "[t]he use of 80 clock cycles...would have been an obvious expedient due to the eighty resultant pixels provided by the 8x10 array" [answer-page 4].

The examiner's rationale, in our view as well as in appellant's, is unreasonable. There is a clear implication in the examiner's rationale that Maruko teaches the writing of one pixel per clock cycle, yet the examiner points to nothing in Maruko, or anywhere else, to support such a position. We agree with appellant that the "mere fact that the art teaches an 8x10 array does not in any way teach or suggestion [sic, suggest] how such array could be updated within eighty clock cycles, as claimed" [brief-page 11, emphasis in original].

We will sustain the rejection of claim 8 under 35 U.S.C. ' 103.

This claim requires the copying of consecutive data words to a range of consecutive addresses and means for receiving the words intended for the range and causing the video controller to actuate "a column of pixels..."

As broadly recited, Diepstraten's graphics processor copies a field of consecutive data words to some range of consecutive addresses and those data words are then used to

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cause a video controller to actuate pixels on a monitor 38. When the graphic is a thin, straight vertical line, the artisan would have recognized that a column of pixels is to be actuated.

On the other hand, claim 9 is not so broad as the subject matter of claim 8 in that the former requires that the means for receiving the data words also distribute those words into VRAM such that the consecutive bytes written by the processor actuate pixels in a single column. Therefore, the language of claim 9 would appear to require that the data words be distributed in a VRAM in a particular manner so as to achieve the particular result of pixel actuation in a single column while claim 8, in contrast, only requires receiving data words and, based on those words, causing the actuation of a column of pixels in no particular manner. While Diepstraten is clearly capable of actuating a column of pixels based on data words from the

processor, there is no suggestion in Diepstraten that that actuation comes about through any particular distribution of the data words in VRAM 30.

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Therefore, while we sustain the rejection of claim 8 under 35 U.S.C. ' 103, we will not sustain the rejection of claim 9 under 35 U.S.C. ' 103.

We have sustained the rejection of claims 2 and 8 under 35 U.S.C. ' 103 but we have not sustained the rejection of claims 1, 3 through 7 and 9 under 35 U.S.C. ' 103. Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR ' 1.136 (a).

AFFIRMED-IN-PART

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