

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

---

Ex parte SAIED ZANGENEHPOUR

---

Appeal No. 95-4899  
Application 08/131,029<sup>1</sup>

---

ON BRIEF

---

Before HAIRSTON, KRASS, and JERRY SMITH, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

---

<sup>1</sup> Application for patent filed October 4, 1993. According to appellant, this application is a continuation of Application 07/918,892, filed July 16, 1992; which is a continuation of Application 07/657,969, filed February 20, 1991; which is a continuation of Application 07/292,189, filed December 30, 1988, all abandoned.

Appeal No. 95-4899  
Application 08/131,029

This is an appeal from the final rejection of claims 14 and 23 through 30.

The disclosed invention relates to a buffer connected between a cache memory and one or more mass storage devices.

Claim 14 is illustrative of the claimed invention, and it reads as follows:

14. In a computer system including a main memory, a central processing unit (CPU), a buffer, a cache memory and one or more mass storage devices, said CPU, main memory and said cache memory being connected to a common bus, said buffer being connected between said cache memory and said one or more mass storage devices, a method of transferring data requested by said CPU between said one or more mass storage devices and said main memory, the method comprising the steps of:

determining whether said requested data is within said cache memory;

transferring a predetermined amount of said requested data from said mass storage device to said buffer when said requested data is not within said cache memory;

transferring a portion of said predetermined amount of said requested data from said buffer to said cache memory while said predetermined amount of said requested data is being transferred from said mass storage device to said buffer; and

transferring a predetermined portion of said requested data from said cache memory to said main memory while said predetermined amount of said requested data is being transferred from said mass storage device to said buffer.

The references relied on by the examiner are:

Appeal No. 95-4899  
Application 08/131,029

Harris et al. (Harris) 1977	4,048,625	Sept. 13,
Ryan et al. (Ryan) 1985	4,551,799	Nov. 5,
Moreno et al. (Moreno) 1988	4,780,808	Oct. 25,

Claims 14, 23 through 25 and 27 through 30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Moreno in view of Harris.

Claim 26 stands rejected under 35 U.S.C. § 103 as being unpatentable over Moreno in view of Harris and Ryan.

Reference is made to the briefs and the answers for the respective positions of the appellant and the examiner.

#### OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 14 and 23 through 30.

At the outset, we note that appellant's extensive arguments concerning the type of buffer used in the disclosed and claimed invention are not convincing of the nonobviousness of the claimed invention because the type of buffer is neither

disclosed nor claimed by appellant (Brief, pages 7 through 14; Reply Brief, pages 4 through 11).

Appellant's acknowledged prior art (specification, page 2) notes that it is well known in the art to use a cache memory between a mass-storage device and a computer because of the differences in processing speeds between the mass-storage device and the computer. Moreno discloses (Figure 1) such a cache memory 30 between a mass-storage device 26 and a host computer 10.

The examiner acknowledges that Moreno discloses only a single cache between the mass-storage device and the host computer, and concludes that Moreno does not need a second one because "[i]t appears that a single cache buffer is sufficient to eliminate data flow problem in Moreno's system" (Answer, page 4).

Harris discloses the use of a first in-first out (FIFO) buffer memory 7 for feeding data to a peripheral device (e.g., printer 6) that processes the data at a much slower rate than the input rate of an input character source 1.

If the data flow problem in Moreno has been taken care of by the cache memory (Answer, page 4), then we see no need to

look to Harris for a teaching of a FIFO buffer to add to Moreno. After all, Moreno never discusses a "peripheral data flow problem" (Answer, page 4), and we are not aware of such a problem in Moreno. Even if we assume for the sake of argument that it would have been obvious to one of ordinary skill in the art to add a FIFO in Moreno, we are not convinced by the examiner's conclusion (Answer, page 4) that "it would have been manifestly obvious to . . . incorporate a FIFO buffer in between the cache memory and the disk of Moreno's system" (emphasis added). Other than appellant's disclosed and claimed invention, nothing in the record would have suggested such a specific location for the buffer.

In summary, the obviousness rejection of claims 14, 23 through 25 and 27 through 30 is reversed because "nothing in the prior art of record suggests incorporating a buffer between a mass storage device and a cache memory" (Brief, page 15).

Ryan discloses a dual or two-part cache memory (Figure 2). A first cache memory 20 handles instruction data, and a second cache memory 22 handles operand data. The data flow through one cache memory is independent of the data flow

Appeal No. 95-4899  
Application 08/131,029

through the other cache memory. Thus, the obviousness rejection of claim 26 is reversed because the independent cache memory teachings of Ryan do not cure the noted shortcomings in the teachings of Moreno and Harris.

Appeal No. 95-4899  
Application 08/131,029

DECISION

The decision of the examiner rejecting claims 14 and 23 through 30 under 35 U.S.C. § 103 is reversed.

REVERSED

	KENNETH W. HAIRSTON	)	
	Administrative Patent Judge	)	
		)	
		)	
		)	
	ERROL A. KRASS	)	BOARD OF
PATENT	Administrative Patent Judge	)	APPEALS AND
		)	INTERFERENCES
		)	
	JERRY SMITH	)	
	Administrative Patent Judge	)	

Appeal No. 95-4899  
Application 08/131,029

KWH/cam

Appeal No. 95-4899  
Application 08/131,029

John S. Paniaguas  
FITCH, EVEN, TABIN & FLANNERY  
135 South LaSalle Street  
Suite 900  
Chicago, IL 60603-4277