THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES J. JIRGAL, DAVID R. EVOY
AND WALTER H. POTTS

Appeal No. 95-5012
Application 08/076,876[1]

ON BRIEF

Before HAIRSTON, JERRY SMITH, and LEE, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 3 through 9, 19, 20 and 23 through 27.

---

[1] Application for patent filed June 11, 1993.

The disclosed invention relates to time shared use of buses within a computer system.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

Claim 1. In a computer system having timed shared use of buses to reduce the number of required pins for devices within said computer system, comprising, in combination:

Central Processing Unit (CPU) means having at least one address bus, at least one data bus, at least one memory input/output, and at least one CPU control bus coupled thereto for sending and receiving information;

at least one memory input/output means coupled to a first portion of said address bus for sending and receiving at least one of address information and data information;

at least one input/output only means coupled to a second portion of said address bus for sending and receiving at least one of address information and data information; and

multiplex system controller means coupled to said CPU means and to said address bus and having multiplex control bus means coupled to both said memory input/output means and to said input/output only means for time sharing said address bus of said CPU means in order to sequentially transfer groups of at least address and data information to said memory input/output means and said input/output only means comprising, in combination:

state machine means coupled to said multiplex control bus means and to said CPU control bus for controlling said multiplex system controller means;

address latch means coupled to said state machine means and to said address bus for temporarily storing address information; and

a plurality of multiplexer means each coupled to said address latch means, said data bus, said state machine means, and to a Direct Memory Access (DMA) controller for transferring data

to said data bus and to said address bus in response to control signals from said state machine means.

The references relied on by the examiner are:

Pohlman et al. (Pohlman)	4,112,490	Sept. 5, 1978
Baker et al. (Baker)	4,286,321	Aug. 25, 1981

Claims 1, 3 through 9, 19, 20 and 23 through 27 stand rejected under 35 U.S.C. § 103 as being unpatentable over Pohlman in view of Baker.

Reference is made to the brief and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1, 3 through 9, 19, 20 and 23 through 27.

With respect to independent claims 1 and 19, the examiner is of the opinion (Final rejection, pages 5 and 6) that:

> Pohlman teaches a CPU connected to a data bus, an address bus, a memory I/O signal line, and a control bus (Figure 2). Pohlman teaches a memory I/O means coupled to a first portion of said address bus (Figure 2). Pohlman teaches an I/O only means (Column 4 lines 28-31), and a multiplex controller as part of his CPU for time sharing said address bus of said CPU in order to sequential [sic, sequentially] transfer groups of at least address and data information to said memory I/O means and said I/O only means (Column 2 lines 24-29). Pohlman teaches a state machine means coupled to said multiplex control bus means and to said CPU control bus for controlling said multiplex system controller means (Control + Timing item 42). Pohlman teaches address

> latch means coupled to said state machine means and to said address bus for temporarily storing address information (item 94 includes address and data buffers as well as multiplexers also Figure 1 item 136). Pohlman also teaches a DMA controller for transferring data to said data bus and to said address bus in response to control signals from said state machine means (Figure 15 item 240, and Column 18 lines 1-25). Pohlman does not teach a plurality of multiplexer means each coupled to said data bus, said address latch, said state machine means, and to the DMA controller. Pohlman only teaches one multiplexer attached to all the items mentioned above.

The computer system in Figure 15 of Pohlman discloses a CPU 20 that has an address bus 48, a multiplexed address/data bus 50, and a control bus 52. A memory I/O device 242 or 262 is connected to all three buses, whereas I/O only peripheral devices are only connected to the multiplexed address/data bus 50 and the control bus 52 via interrupt controller 238. A DMA 240 is shown connected between the CPU and the three buses. Pohlman states (column 5, lines 20 through 25) that a state generator is part of the timing circuitry portion 30 of the CPU 20 (Figure 1). In Figure 2 of Pohlman, latches 244 and 264 are shown as part of memory I/O devices 242 and 262, respectively.

We agree with the examiner that Pohlman discloses a state machine means, an address latch means, a DMA controller, and a multiplexer (not shown) in CPU 20 to handle the time multiplexing between address and data on bus 50, but we do not, however, agree

with the examiner that such structure is connected in a computer system in the manner required by the claims on appeal. For example, Pohlman does not have a multiplex system controller means with a multiplex control bus connected to the memory input/output means and the input/output means for time sharing the address bus of the CPU in order to sequentially transfer groups of at least address and data information. If such a multiplex system controller is not in Pohlman's system, then Pohlman cannot have a "state machine means coupled to said multiplex control bus means and to said CPU control bus for controlling said multiplex system controller means," and "address latch means coupled to said state machine means and to said address bus for temporarily storing address information" (Claims 1 and 19) (Brief, page 9).

Even if we assume for the sake of argument that it would have been obvious to one of ordinary skill in the art to modify Pohlman in accordance with Baker to use a plurality of multiplexers in lieu of a single multiplexer (Final rejection, page 6), we are still left with the fact that the combined reference teachings would still lack the specifically claimed computer structure set forth in the claims on appeal. Thus, the obviousness rejection is reversed.

DECISION

The decision of the examiner rejecting claims 1, 3 through 9, 19, 20 and 23 through 27 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
JAMESON LEE Administrative Patent Judge	)

VLSI TECHNOLOGY, INC.
Legal Department
1109 McKay Drive
San Jose, CA 95131