

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WILLIAM O. McDERMITH
MEHRDAD BANKI,
and KEVIN M. BUSH

Appeal No. 96-0137
Application 08/074,978¹

ON BRIEF

Before URYNOWICZ, HAIRSTON and LEE, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 9-14, all the claims pending in the application.

¹ Application for patent filed June 10, 1993. According to applicants, this application is a continuation of Application 07/782,288, filed October 24, 1991, now abandoned, which is a continuation of Application 07/294,470, filed January 6, 1989, now U. S. Patent No. 5,140,526, granted August 18, 1992.

The invention pertains to partitioning of Boolean logic equations into physical logic devices. By way of example, the invention involves the selection of the most appropriate commercially available interface circuit devices from a data base that allow a peripheral device to communicate with a computer or another interface device. Claim 11 is illustrative and reads as follows:

11. An automated partitioning method for implementing, on a processor, a given set of Boolean logic equations to one or a plurality of discrete manufactured physical logic devices, each of said discrete manufactured physical logic devices having an architectural type number, pins, pin assignments, manufacturer identity, model number, and price, said processor connected to an input, a memory, and an output, said method comprising the steps of:

storing template information on different architectural types of said discrete manufactured physical logic devices in a template file of said memory of said processor in response to receiving said template information from said input, said template information at least providing one of the following said architectural type number, number of said pins, and said pin assignments,

storing device information corresponding to each said different architectural type number in a device information file of said memory of said processor in response to receiving said device information from said input, said device information at least providing one of the following said manufacturer identity, said model number, and said price,

storing selected user constraints for said device selection in a criteria file in said memory of said processor in response to receiving said constraints from said input, said constraints defining selection limits for said device information,

storing selected user partitioning directives for said device selection in a partitioning directives file in said memory of said processor in response to receiving said partitioning directives from said input, said partitioning directives defining predetermined physical relationships for partitioning of said Boolean logic equations,

automatically identifying from the stored template and the stored user constraints in said memory, via said processor and independent of said input, in a possible solutions list in said

memory, all discrete manufactured physical logic devices that have (1) a template of an architectural type wherein at least one of said Boolean logic equations in said set fits and (2) an information file wherein all said selected user constraints are met,

automatically ordering, via said processor, independent of said input and receptive of said possible solutions list from said step of identifying, the discrete manufactured physical logic devices contained in said possible solutions list into an ordered possible solutions list,

automatically fitting from the stored selected user partitioning directives from said memory, via said processor, independent of said input and receptive of said ordered possible solutions list, each of said Boolean equations to each of said discrete manufactured physical logic devices in said ordered list of possible solutions according to said partitioning directives, said step of fitting comprising the steps of:

(i) trying to fit the pins and pin assignments of each device in said ordered possible solutions list to said set of Boolean equations,

(ii) adding only those devices that fit in the aforesaid step (i) to a device solution list,

mapping, via said processor, said set of Boolean equations onto the discrete manufactured physical logic devices in said list of device solutions.

The references relied upon by the examiner as evidence of obviousness are:

LOGIC/iC software, PLD Compiler Manual, ISDATA GmbH, Haid-und-Neu-StraBe 7, D-7500 Karlsruhe, West Germany, copyrighted 1987 & 1988.

“PLD-design software meets the challenge of multiple-device PLD applications”, Small, Charles H., EDN, vol. 33, no.4, Feb. 18, 1988, pages 61-65.

APS Text Search and Retrieval Manual, Planning Research Corporation, 1986 revision, pages 2-9, 4-3 and 4-4.

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HP PLDDS Standard Utilities, HP Part Number 74150-90905, Hewlett-Packard Company, copyright 1988.

LOG/iC Design Made Easy, ISDATA Inc., 06/88, 4 sheets provided by appellants in the 7/20/93 information disclosure statement (Paper No. 14).

LOG/iC data sheets, ISDATA Inc., 11/88, 6 sheets provided by appellants in the 7/20/93 information disclosure statement (Paper No. 14).

Claims 9-12 stand rejected under 35 U.S.C. § 103 as unpatentable over LOG/iC software, PLD Compiler Manual, in view of Small.

Claims 13 and 14 stand rejected under 35 U.S.C. § 103 as unpatentable over LOG/iC software, PLD Compiler Manual, in view of Small and the APS manual.

The respective positions of the examiner and the appellant with regard to the propriety of these rejections are set forth in the final rejection (Paper No. 22) and the examiner's answer (Paper No. 30) and the appellant's brief (Paper No. 29).

With respect to the prior art relied on by the examiner to reject claims 9-14, appellants make no argument that there is no motivation to combine the teachings in that art. Rather, appellants take a position to the effect that the combined art is deficient in a number of ways. Appellants' position is to the effect that, although the prior art discloses apparatus and methods for selecting one or more electronic devices from a plurality of commercially available devices, the prior art does not disclose additional, specific features of their invention.

The Rejection under 35 U.S.C. §103

Claims 9-12

With respect to claims 9-12, appellants contend that the following specific features of the claims establish their unobviousness. Appellants argue that “LOG/iC’s PLD Database program” of the LOG/iC PLD Compiler Manual does not provide for a price information feature. Appellants contend that the art applied by the examiner teaches manual partitioning, not the required automatic partitioning. According to appellants, “fitting”, as taught in their application and as claimed, means automatically assigning input and output pins to the device in such a manner as to provide a means of successfully implementing a design into a selected device, and the prior art does not teach automatic “fitting”. Lastly, appellants contend that the prior art does not teach producing a list of devices that comprises an ordered list of solutions.

After consideration of the positions and arguments presented by appellants, we have concluded that the rejection of claims 9-12 should be sustained. With respect to appellants’ first argument, noted above and related to pricing information, in the reference to Small in the paragraph bridging sheets 3 and 4, it is disclosed that “HP’s HP PLD and Minc’s Logic Designer take into consideration such device-specific factors as power consumption, pricing, and inventory restrictions when making an automatic device selection. As to appellants’ second and third arguments, in the first full paragraph of the second sheet of Small, it is disclosed that software packages that can select devices and partition

designs automatically are known and in the fourth full paragraph of the third sheet it is disclosed that “Kontron’s LOG/iC can automatically select devices and partition your design”². The utilization of price information, and automatic partitioning and fitting, in LOG/iC software, PLD Compiler Manual, based on the above teachings in Small would have been obvious to one of ordinary skill in the art at the time appellants’ invention was made. Section 103 requires us to presume that the artisan has full knowledge of the prior art in his field of endeavor and the ability to select and utilize knowledge from analogous arts. In re Deminski, 796 F.2d 436, 442, 230 USPQ 313, 315 (Fed. Cir. 1986). This is even more true with respect to like art such as applied by the examiner here.

In his answer, the examiner also relies on page C2 of the HP PLDDS Standard Utilities document in responding to appellants’ arguments³. The manual is relied on to establish that pin assignment is automatically generated in a system for device selection of the type at issue here. This teaching is cumulative with respect to what is taught in the reference to Small and we agree with appellants that what the manual teaches with respect to pin selection is not fully automatic but only semi-automatic since the user of the system must manually click on a displayed icon. However, we agree with the examiner’s alternate position that it would have been obvious to one of ordinary skill in

² In their Fig. 4, appellants disclose that one of the three main partitioning processes is fitting. In their brief, appellants assert fitting involves device pin assignments. In the third full paragraph of its third sheet, the Sm reference discusses pin assignment in connection with the partitioning process.

³ Although this manual is not included in the examiner’s statement of the rejection, we will treat it as so included as it was relied on by the examiner in his final rejection and argued by appellants in their brief.

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the art at the time the invention was made to provide automatic means to

initiate the fitting or pin selection function to replace the manual activity. In re Venner, 262 F.2d 91, 120 USPQ 192 (CCPA 1958).

Appellants' argument that the solution list of the prior art is not ordered is not persuasive. We agree with the examiner that none of claims 9-12 recites such a list. The argument is simply not commensurate in scope with the claims⁴.

The Rejection under 35 U.S.C. § 103

Claims 13 and 14

In their brief appellants take a position to the effect that the prior art does not teach a partitioning file memory for storing user partitioning directives as recited in claims 13 and 14. The examiner is silent with respect to the existence of such a memory in the prior art.

We will not sustain this rejection. By not addressing the above limitation, the Patent Office has not fulfilled its burden of establishing prima facie obviousness of the claimed subject matter. The burden

⁴ Even if the claims recited an ordered solution list, they would not appear to be directed to allowable subject matter. At the last paragraph of page C1 of the HP PLDDS Standard Utilities Manual, it is disclosed that PLDDS presents a window of numbered usable devices in the order of their usefulness. Such a window constitutes an ordered solution list.

We have not referred to the last two references which are indicated above as relied on by the examiner. These references do not appear to teach anything concerning the production of an ordered solution list of useable devices beyond that taught by the HP PLDDS Standard Utilities Manual.

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is upon the Patent Office to show prima facie obviousness. In re Piasecki, 745 F.2d 1468, 1471-72,
223 USPQ 785, 788 (Fed. Cir. 1984).

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Summary

In summary:

- a) the decision of the examiner to reject claims 9-12 under 35 U.S.C. § 103 is affirmed.
- b) the decision of the examiner to reject claims 13 and 14 under 35 U.S.C. § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

STANLEY M. URYNOWICZ, JR.)
Administrative Patent Judge)
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) BOARD OF PATENT
KENNETH HAIRSTON) APPEALS AND
Administrative Patent Judge) INTERFERENCES
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