

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YOUNG W. LEE,
SUNGWON MOH and
ARNO MULLER

Appeal No. 96-0982
Application 08/163,812¹

ON BRIEF

Before JERRY SMITH, BARRETT and FLEMING, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed December 9, 1993.

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This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claim 8, which constitutes the only claim remaining in the application. An amendment after final rejection was filed on February 6, 1995 but was denied entry by the examiner [Paper #6].

The disclosed invention pertains to an improved control system for a postage meter. Specifically, the invention is directed to the manner in which memory enable signals are applied to memories having different access times.

The single claim on appeal is reproduced as follows:

8. An improved electronic postage meter control system having a printing means including means for printing mixed graphic and alphanumeric information in response to said control circuit, said control circuit including a programmable microprocessor in bus communication with said printing means for controlling said printing means and with a plurality of memory units for accounting for postage printed by said printing means, said memory units including at least a first memory unit having a write access time shorter than the write access time of a second one of said memory unit, a program memory means in bus communication with said programmable microprocessor having an operating program stored therein, said programmable microprocessor being able to access said operating program, an integrated circuit in bus communication with said programmable microprocessor, said program memory, and said first and second units, wherein said improvement comprises:

said integrated circuit having an address decoding module means for generating one of a plurality control signals in a unique combination in response to a respective address

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evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the disclosure of Larson does not fully meet the invention as set forth in claim 8. Accordingly, we reverse.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

In the rejection of claim 8, the examiner notes that Larson discloses application specific integrated circuits (ASICs) to provide control and timing signals to components of his system. Since the postage meter of claim 8 was admittedly old, the examiner asserts that "it would have been inherent to one of ordinary skill at the time the invention was made that an ASIC could be used to provide the correct timing and interfacing signals in any computer system, such as the claimed postage metering system" [answer, page 2].

Appellants respond that the address decoding module means, the means for maintaining and the second means for maintaining as recited in claim 8 are not disclosed in Larson. Specifically, appellants argue the following:

The ASIC address decoder (28) when it receives a valid address from the microprocessor (15) generates the appropriate chip select and write or read enable signal enabling access to the appropriate memory. If the selected memory is one of the NVMs, the respective chip select signal is directed not only to the NVM enable pin but also to a delay circuit (66 or 66E). The delay circuit delays the generation of a DTACK signal for a desired time which is sufficiently long enough to assure a completed

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memory access of the NVM unit selected
[brief, page 4].

Thus, appellants argue that there is no disclosure in Larson of a method whereby the write enable signals are held active as a result of a delay circuit nor is there anything inherent which would imply using a wait state system responsive to ASIC control signals.

The examiner responds again that the claimed operation is inherent in Larson and that there is no recitation of a delay circuit in claim 8 [answer, pages 3-4]. Appellants respond that the examiner's assumptions to support his inherency argument are contrary to the conventional practice in the art [reply brief].

When we consider the rules of claim construction and the requirements of a reference under 35 U.S.C. § 102, we agree with appellants that the examiner has failed to demonstrate that the invention of claim 8 is fully met by the disclosure of Larson.

Claim 8 is drafted as an apparatus claim in means plus function form as authorized by the last paragraph of 35 U.S.C.

§ 112. The plain and unambiguous meaning of this paragraph is that one construing means-plus-function language in a claim must look to the specification and interpret that language in light of the corresponding structure, material, or acts described therein, and equivalents thereof, to the extent that the specification provides such disclosure. In re Alappat, 33 F.3d 1526, 1540, 31 USPQ2d 1545, 1554 (Fed. Cir. 1994); In re Donaldson, 16 F.3d 1189, 1193, 29 USPQ2d 1845, 1850 (Fed. Cir. 1994). As noted above, appellants point to the apparatus of Figure 2 as performing the functions of the address decoding means, the means for maintaining and the second means for maintaining. This structure includes logic circuitry in combination with a delay circuit (66 or 66E). Therefore, the proper interpretation of claim 8 includes a delay circuit as shown in Figure 2, and it was improper for the examiner to argue that there was no delay circuit being claimed.

Since the examiner has not properly interpreted the structure of the invention as recited in claim 8, the examiner has failed to demonstrate that the apparatus specifically recited in claim 8 is fully met by the disclosure of Larson. We also find no basis to accept the examiner's bare allegation

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that the apparatus of claim 8 is inherently present in the Larson device. The examiner's position is nothing more than a statement that the structure of Larson is capable of achieving the result desired by appellants' invention, but the examiner has failed to demonstrate that the result in Larson is achieved by inherently using the specific structure recited in claim 8.

For all the reasons discussed above, the examiner's rejection of claim 8 under 35 U.S.C. § 102 is reversed.

REVERSED

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JERRY SMITH)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT))
Administrative Patent Judge)	APPEALS AND
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)	INTERFERENCES
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