

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEITH BALMER

Appeal No. 96-1014
Application 08/032,530¹

ON BRIEF

Before JERRY SMITH, BARRETT, and HECKER, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from

¹ Application for patent filed March 15, 1993, entitled "Synchronized MIMD Multi-Processing System And Method Of Operation," which is a continuation of Application 07/437,853, filed November 17, 1989, now abandoned.

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the final rejection of claims 23-44, which constitute all of the pending claims.

We affirm-in-part.

BACKGROUND

The disclosed invention is directed to an apparatus and method for operating a plurality of processors in synchronism, as described with respect to figures 21-23 in the section of the specification at pages 38-44 entitled "Synchronized MIMD."

Claim 35 is reproduced below.

35. The method of operating a computer system having a plurality of processors in synchronism, each of the processors independently fetching and executing instructions, said method comprising the steps of:

storing at each processor an indication of other processor or processors to which said processor is to be synchronized;

generating at each processor a ready signal when said processor is ready to fetch an instruction;

inhibiting fetching an instruction at each processor until said processor receives said ready signal from all other processor or processors to which said processor is to be synchronized according to said stored indication and thereafter fetching said instruction at each processor; and

executing fetched instructions at each processor, whereby each processor is synchronized with said other

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processor or processors according to said stored indication on an instruction by instruction basis.

The examiner relies on the following prior art patents:

Jaswa	4,733,353	March 22,
1988		
Kametani	5,107,420	April 21,
1992		
		(filed August 13,
1987)		

Claims 23-44 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kametani and Jaswa.

We refer to the Final Rejection (Paper No. 20), the Examiner's Answer (Paper No. 26) (pages referred to as "EA__"), the [First] Supplemental Examiner's Answer (Paper No. 28) (pages referred to as "SEA__"), and the [Second] Supplemental Examiner's Answer (Paper No. 28 on paper, but No. 30 on file wrapper) (pages referred to as "2dSEA__") for a statement of the examiner's position. We refer to the Appeal Brief (Paper No. 25) (pages referred to as "Br__"), the Reply Brief (Paper No. 27) (pages referred to as "RBr__"), the Supplemental Reply Brief (Paper No. 29) (pages referred to as "SRBr__"), and the Second Supplemental Reply Brief (Paper No. 31) (pages referred to as "2dSRBr__") for a statement of appellant's position.

OPINION

Grouping of claims

The examiner's statement (EA2) that appellant has not presented arguments in support of the independent patentability of identified groups of claims is in error. Appellant has argued the separate patentability of claims 23, 26-30, 33-35, 39, 43, and 44.

Obviousness

We find the references to be representative of the level of ordinary skill in the art. See In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("the PTO usually must evaluate both the scope and content of the prior art and the level of ordinary skill solely on the cold words of the literature"); In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (the Board did not err in adopting the approach that the level of skill in the art was best determined by the references of record). Obviousness is determined through the eyes of one of ordinary skill in the art and one of ordinary skill in the art must be presumed to know something about the art apart from what the references expressly disclose. See

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In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA 1962); In re Oetiker, 977 F.2d 1443, 1447-48, 24 USPQ2d 1443, 1446-47 (Fed. Cir. 1992) (Nies, C.J., concurring). We find that the level of ordinary skill in the pertinent art of designing synchronized processors is very high and involves extensive knowledge of computer architecture, logic design, and software.

Claims 23-25 and 35-38

Kametani discloses an apparatus for synchronizing processors which is markedly similar to appellant's apparatus in figure 22. Kametani has a signal line 8 corresponding exactly to appellant's synchronization bus 40; a synchronous register 5 corresponding exactly to appellant's sync register 2207; and a monitoring circuit 6 (shown in more detail in figure 2) corresponding exactly to appellant's synchronization logic gates 2202-2206. The trigger signal 10 in Kametani corresponds to appellant's EXECUTE signal. In Kametani, the pulse on signal line 4 from the processor to the flip-flop 7 and the resulting "0" on the terminal Q of the flip-flop 7 correspond to appellant's claimed "okay to synchronize" signal. Kametani

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differs from the disclosed structure from appellant's figure 22 in its use of a flip-flop 7 to generate the "okay to synchronize" signal instead of a NAND gate 2201. It is true, as noted by appellant (RBr3-4), there are differences in the way the Kametani's circuitry works because of the flip-flop; however, the issue is whether any claimed differences would have been obvious.

Appellant argues (Br5), with respect to claims 23 and 35, that the combination of Kametani and Jaswa fails to teach or suggest: (1) synchronization "on an instruction by instruction basis"; and (2) inhibiting the fetching of instructions until each processor has transmitted a signal that the processor is ready to synchronize and then fetching and executing an instruction, which is carried out with a "program counter register" in apparatus claim 23.

As to synchronization "on an instruction by instruction basis," appellant argues (Br6): "First, Kametani fails to disclose instruction by instruction synchronization and specifically teaches task synchronization that may take differing times. Second, Jaswa mentions instruction by instruction synchronization, but states that this is

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disadvantageous compared with frame by frame
synchronization."

Kametani discloses task by task synchronization. The examiner states that "[a] 'task' as understood in the art can be a single instruction" (EA4) and "[a] task includes one or more instructions" (EA5). We agree that one of ordinary skill in the pertinent art of synchronizing processors would have had sufficient knowledge to appreciate that the task in Kametani could be a single instruction or a group of instructions. Obviousness is determined through the eyes of one of ordinary skill in the art and is not based just on the express teachings of the references.

The examiner further applies Jaswa for its teaching that "[i]nstruction synchronism is a widely used synchronization technique" (col. 1, lines 34-35). Jaswa also discloses that instruction synchronization has disadvantages in synchronizing multiply redundant computers; however, this does not negate the teaching that instruction by instruction synchronization was a widely used technique. We agree with the examiner that the teaching of instruction by instruction synchronization in Jaswa would have motivated

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one having ordinary skill in the art of synchronizing processors to make the task in Kametani a single instruction.

The examiner's statement that "what is different between instruction synchronization and task synchronization is only the label" (EA6) is inaccurate because a task could be a single instruction or a group of instructions. Synchronizing the beginning and end of a task does not imply that instructions within the task are synchronized on an instruction by instruction basis. Appellant's response to the statement (RBr4-6) focusses on the single instruction disclosure of the application, which is not in question. Appellant also argues that figure 5 of Kametani shows tasks 11 and 12 beginning at a different time t_4 than tasks 9 and 10 which begin at time t_3 , and that "[t]hese different starting times for synchronized tasks cannot take place in the present invention" (RBr6). We disagree with appellant's interpretation of figure 5. While all tasks in a group, e.g., group 15, are associated (col. 4, lines 5-8), they are not all synchronized if the tasks are independent; i.e., processors a and b are synchronized at time t_3 and

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processors c and d are synchronized (to each other and not to processors a and b) at time t_4 . Where a group of processors is synchronized, they start and end the task at the same time; e.g., processors a, b, and d are synchronized at time t_5 and end the task at time t_6 . Thus, Kametani is not inconsistent with the task being a single instruction.

As to the limitations of inhibiting the fetching of the next instruction until a ready signal is received from each processor to be synchronized and then fetching and executing the next instruction, Kametani admittedly does not expressly disclose that this is what happens or that a program counter is used. Kametani describes that processing by the processor is interrupted until the TEST input becomes "0" in response to all the processors to be synchronized having indicated that they have ended their task and are ready to be synchronized, whereupon the processor starts processing again (col. 2, line 65 to col. 3, line 1; col. 3, lines 16-25). Impliedly, the processor starts processing by fetching and then executing the next instruction. The examiner finds that program counters are inherent in computers and that Kametani's interruption and continuation

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of processing would necessarily operate by inhibiting and then permitting fetching and executing using a program counter (EA4). Appellant does not appear to contest this reasoning. We agree that stored program computers use program counters to store the address of the next instruction to be executed. Although some evidence from the examiner would have been preferable, in our opinion, one of ordinary skill in the art of synchronizing processors would have known that one way to interrupt and continue the processing in Kametani would have been to inhibit the fetching of the instruction in the program counter and then permit fetching and executing of the next instruction in the program counter. This reasoning is based on obviousness, not inherency.

For these reasons, we sustain the rejection of claims 23 and 35, and also dependent claims 24, 25, and 36-38, which have been grouped to stand or fall with claims 23 and 35.

Claims 26-34 and 39-44

Claim 30 recite a "synchronization flag memory having stored therein an indication of whether said processor is in

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a synchronized mode or in an unsynchronized mode" which is connected to the synchronization logic unit, and the synchronization logic unit permits "the fetching of the next instruction by said program counter register regardless of the status of said synchronization bus and said synchronization register when said synchronization memory flag indicates said unsynchronized mode." Claim 26 contains similar limitations. Process claim 39 recites "storing at each processor an indication of a synchronized mode or an unsynchronized mode" and "permitting fetching an instruction at each processor regardless of the status of the ready signal of the other processors when said processor stores an indication of the unsynchronized mode." Appellant argues that this "permits changing a processor between synchronized and unsynchronized modes without changing the indication of which processors that the processor is to be synchronized [with] stored in synchronization register 2207" (Br7).

The examiner states (EA9):

Jaswa on column 2 line 17 shows setting a synch flag when synchronized operations are to be performed. Please note that this flag is set only when synchronization mode is selected, as mentioned above. Also, on column 1, lines 34-53 Jaswa states that it is desirable to run the processors asynchronously between

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synchronizations. Fetching an instruction regardless of the status of the synchronization bus necessarily follows when unsynchronized mode of operation is indicated since this indicates asynchronous operation. In other words when the synch flag is not set, asynchronous operation occurs.

Jaswa discloses that in frame synchronization techniques "the processing systems are synchronized only periodically at some predetermined frame interval and are permitted to run asynchronously between synchronizations" (col. 1, line 46-49). Jaswa also discloses that each computer system is instructed "to set a sync flag" (col. 2, line 17). Appellant argues that the sync flag in Jaswa and the flip-flop 7 in Kametani are equivalent to the "okay to synchronize" signal of this invention (RBr8-10). We have studied Jaswa and the examiner's arguments in response and agree with appellant. The sync signal causes a frame synchronization to occur, just as the "okay to synchronize" signal of this invention and the "0" output of the flip-flop 7 in Kametani; it does not act as a flag to turn instruction by instruction synchronization between processors off and on. In our opinion, the teaching of synchronized and unsynchronized modes of operation and a sync flag in Jaswa would not have motivated one of ordinary skill in the art to

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modify Kametani to arrive at the claimed synchronization flag memory.

Appellant correctly notes that "[i]n Kametani a processor may be placed in a mode not synchronized with any other processor by writing all zeros into synchronous register 5 of Figure 1" (Br8). Appellant argues that "[t]he synchronization flag memory recited in claim 30 is clearly a different structure than the synchronization register" (Br9). We agree. The processors in Kametani can be run unsynchronized, but this does not meet the synchronization flag memory limitation.

Appellant argues that the examiner failed to point out a flag memory or software setting of the flags in Kametani or Jaswa in the Final Rejection or the Examiner's Answer (e.g., Br9, RBr10). The examiner responds (SEA6): "It is submitted that the appellant argues details which are not critical such as whether there is a memory to store a flag and/or whether an instruction sets the flag or the hardware sets the flag and obscure the invention which is selective synchronization of the processors using the registers as shown in Kametani." We agree with appellant's response

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(SRBr4) that the language of the claims is always relevant. Assuming, arguendo, that Kametani provides the same end result through some undisclosed combination of software and hardware, this is not probative on the obviousness question since different structures to produce the same result may be separately patentable. It is the subject matter of the claims that must be examined for patentability. See In re Wilder, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970)("[E]very limitation positively recited in a claim must be given effect in order to determine what subject matter that claim defines."). We conclude that the examiner has failed to establish a prima facie case of obviousness with respect to the synchronization flag memory of claims 26 and 30, and the step of storing at each processor an indication of a synchronized mode or an unsynchronized mode in claim 39. Therefore, we reverse the rejection of claims 26-29, 30-34, and 39-44.

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CONCLUSION

The rejection of claims 23-25 and 35-38 is sustained.

The rejection of claims 26-34 and 39-44 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

	JERRY SMITH)	
	Administrative	Patent Judge)
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)	BOARD OF
PATENT)	
	LEE E. BARRETT)	APPEALS
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