

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GREGORY S. VASCHE

Appeal No. 96-1207
Application No. 08/064,203¹

ON BRIEF

Before HAIRSTON, BARRETT and FRAHM, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 13, 14, 16, 17 and 19 through 25.

The disclosed invention relates to an integrated circuit device, and to a method of depositing a tunneling oxide layer

¹ Application for patent filed May 21, 1993. According to the appellant, the application is a division of Application No. 07/545,122, filed June 26, 1990, now Patent No. 5,219,774, which is a continuation of Application No. 07/195,766, filed May 17, 1988.

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between two conductive layers of the device. In the method of depositing the tunneling oxide, a silicon dioxide layer is formed by a low pressure chemical vapor deposition (LPCVD) process using tetraethylorthosilicate (TEOS). After the tunneling oxide is deposited, it is subjected to an annealing step.

Claims 13 and 14 are the only independent claims on appeal, and they read as follows:

13. An improved tunneling region for use with an integrated circuit comprising:

a first layer of polysilicon;

a first electron tunneling layer of thermal oxide formed over said first layer of polysilicon;

a second electron tunneling layer of annealed deposited silicon dioxide formed over said first tunneling layer having a thickness less than 2000 Angstroms thick, said silicon dioxide layer being formed by low pressure chemical vapor deposition comprising the use of tetraethylorthosilicate; and

a second layer of polysilicon formed over said layer of deposited silicon dioxide, such that when a bias voltage is applied between said first layer of polysilicon and said second layer of polysilicon, electron tunneling will occur from said first layer of polysilicon to said second layer of polysilicon through said first and second electron tunneling layers.

14. A semiconductor device including means for electron tunneling, comprising:

a first conductive layer;

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an annealed silicon dioxide tunneling layer having a thickness less than 2000 Anstroms formed on top of said conductive layer, said silicon dioxide layer being formed by low pressure chemical vapor deposition comprising the use of tetraethylorthosilicate;

a second conductive layer formed on top of said silicon dioxide layer, said first conductive layer acting as a source of tunneling electrons under an appropriate voltage bias condition, said second conductive layer serving as the receptor of said tunneling electrons.

The references relied on by the examiner are:

Sato	4,720,323	Jan. 19, 1988
Hazani	4,763,299	Aug. 9, 1988

Korma et al. (Korma), "SiO₂ Layers on Polycrystalline Silicon," Insulating Films on Semiconductors, Proceedings of the International Conference, Elsevier Science Publishers, 1983, pages 278 through 281.

Claims 13, 14, 16, 17 and 19 through 25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hazani.

Claims 13, 14, 16, 17 and 19 through 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sato in view of Korma.

Reference is made to the briefs and the answer for the respective positions of the appellant and the examiner.

OPINION

All of the rejections are reversed.

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There is no dispute that the applied references disclose all of the claimed structure. The only issue on appeal is the weight to be given to the process step of "said silicon dioxide layer being formed by low pressure chemical vapor deposition comprising the use of tetraethylorthosilicate" in each of the claimed products. It is the examiner's position (Answer, page 4) that:

With regard to the process limitations within Claims 13, 14, and 16, the applicant is reminded that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. See *In re Thorpe*, 227 USPQ 964.

In assessing the patentability of product-by-process claims, the Court stated in *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972) that:

[T]he lack of physical description in a product-by-process claim makes determination of the patentability of the claim more difficult, since in spite of the fact that the claim may recite only process limitations, it is the patentability of the *product* claimed and *not* of the recited process steps which must be established. We are therefore of the opinion that

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when the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claimed in a product-by-process claim, a rejection based alternatively on either section 102 or section 103 of the statute is eminently fair and acceptable.

Inasmuch as all of the product limitations are disclosed by the applied prior art, the examiner has established a prima facie case of unpatentability of the claimed invention.

Notwithstanding the prima facie case of unpatentability, the appellant can come forward with evidence establishing an unobvious difference between the claimed product produced by the process recited supra and the prior art product produced by a conventional process. In re Marosi, 710 F.2d 799, 803, 218 USPQ 289, 292-93 (Fed. Cir. 1983).

The evidence submitted by appellant is three declarations attached to the brief as Exhibit A through C. The three declarations are executed by William H. Owen, Vice President, Product Planning and Intellectual Properties, Xicor, Inc., the assignee of the subject patent application. The three declarations make clear that the unobvious differences between the claimed process and the conventional processes are discussed throughout the specification. In the Exhibit A declaration, for example, paragraph 10 discusses the portion

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of the disclosure that states that "[t]he process of the present invention has been found to increase the total charge conducted through the dielectric layer by at least one order of magnitude before catastrophic breakdown, while at the same time providing a dramatic improvement in processing yields" (specification, pages 6 and 7). In paragraph 20 of this same declaration, declarant states that:

I consider the annealing process developed by Vasche as being a very important aspect of his invention. As is explained in the specification at page 6, the unique annealing process results in a TEOS oxide layer with substantially improved dielectric properties, better leakage properties and better breakdown properties than what was known in the prior art. The improvements that were realized in respect to these properties by performing a new annealing process were completely different from what was known in the prior [art]. In my opinion, these results were truly surprising.

Paragraph 6 in the Exhibit B declaration states that:

[T]he devices claimed in the present invention all use the CVD deposited layer as a *tunneling layer* (i.e., a layer through which tunneling electrons flow to program or erase the floating gate), not simply as a[n] insulating layer. As I pointed out in my prior Declaration, such a tunneling layer must have both good insulating properties and good tunneling properties to be useful in a floating gate memory device. The present patent application teaches the surprising result that a properly deposited and annealed TEOS

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layer is both an insulator suitable for floating gate memory devices as well as an improved tunneling layer. Neither of these properties have been previously taught in any prior art I am aware of.

The noted enhancement of electron tunneling is described in the specification at page 4, lines 29 through 35.

In paragraph 6 of the Exhibit C declaration, declarant states that:

Mr. Vasche's work at Xicor significantly advanced the state of the art in the field of non-volatile memories. He found that low temperature deposited dielectrics, properly annealed, are better than thermal oxides for tunneling. For example, as stated in the specification, beginning at the bottom of page 6, the inventor discovered that TEOS tunneling oxides formed in the manner claimed in this case increase the total charge which can be conducted through a dielectric layer by at least an order of magnitude while at the same time providing a dramatic improvement in processing yields.

Paragraphs 8 and 9 of the Exhibit C declaration are as follows:

The structure of the tunneling oxide layer according to the present invention is significantly different from prior art tunneling oxide layers since the inventive layer is substantially free of stress and defects. See page 4 line 23 to page 5, line 4 of the specification.

More specifically, first with regard to defects, when the claimed TEOS deposited oxide layer is being deposited, it does not consume the underlying layer, as is well known in the art. Thermal oxide, however, as is also well known, does consume the underlying layer,

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and the resultant defect density of the thermal oxide layer is directly dependent on the underlying defect density of the material on which the oxide layer is formed. For example, pinholes are often created in a thermal oxide layer as a result of small metallic impurities in the underlying silicon or polysilicon layer. The TEOS deposited layer coats all surfaces and thus will fill in such pinholes (so long as the defects are smaller than the thickness of the TEOS layer).

The propagation of defects in the polysilicon layer into the thermally grown tunneling oxide layer leads to stress and defects

in the conventional tunneling oxide layer as discussed at page 4, lines 16 through 22 of the specification.

The issue of stress is also addressed in paragraph 10 of the Exhibit C declaration as follows:

With regard to the issue of stress, it is well known that stress is induced in a wafer when a thermal oxide layer is grown. The induced stress can be large enough to cause warping of the wafer. . . . It is well known that [a] TEOS deposited layer can be defined to induce either compressive or tensile stress, and be of a much lower magnitude than for thermally grown oxide. Consequently, stress can be minimized when using a TEOS deposited tunneling oxide layer. This provides the advantage of a device having a much greater useful life.

Declarant summarizes his position in paragraph 12 of this same declaration by stating that:

Although the structure of the dielectric layer created according to the present invention is clearly different from prior art thermal oxide layers, it is not possible in my opinion to describe it except in terms of the process for making this structure. As stated in the specification, in addition to the above differences in defect density and stress between thermal and TEOS deposited oxides, the annealing of the TEOS layer seems to provide a more uniform molecular bonding by permitting greater viscous flow in the TEOS deposited oxide thus reducing or eliminating defects in the resulting dielectric layer. The result is, as stated in the specification, a dielectric layer that enables an increase of at least one order of magnitude in the total charge conducted through the dielectric layer, while at the same time providing a dramatic improvement in processing yields. The structure must be different in order to obtain this effect, but it is not currently within the state of the art to describe in physical terms how this structure is different from an oxide layer formed entirely by thermal oxidation.

The foregoing advantages of TEOS deposited oxides versus thermally grown oxides can be found in the specification at page 6, line 12 through page 7, line 1.

As indicated supra, the advantages of appellant's claimed process step are set forth in the declarations as well as in the specification.² Such advantages are sufficient to establish unobvious differences between the claimed product and

² A patent application and a declaration are both under oath.

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the prior art product described in the applied prior art. In summary, the prima facie case of unpatentability established by the examiner has been successfully rebutted by the appellant. Thus, all of the rejections are reversed.

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DECISION

The decision of the examiner rejecting claims 13, 14, 16, 17 and 19 through 25 under 35 U.S.C. § 102(b) and 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	
)	
)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
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