THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 40

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte TOSHIHIRO OHBA, ATSUSHI SAKAMOTO, YOSHIYUKI KOKUHATA, HIROSHI KISHISHITA and HISASHI UEDE

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Appeal No. 96-2025
Application 07/860,254[1]

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HEARD: March 10, 1999

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Before THOMAS, FLEMING, and LALL, Administrative Patent Judges.

FLEMING, Administrative Patent Judge.

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[1] Application for patent filed March 31, 1992. According to the appellants, the application is a continuation of Application 07/443,391, filed November 30, 1989, now abandoned.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 9, all of the claims present in the application.

The invention relates to a method and an apparatus for driving display devices such as an ac driven capacitive flat matrix display panel. On page 20 of the specification, Appellants disclose that Figure 6 shows the waveform of the voltage applied to a corresponding picture element. In particular, Figure 6 (1) shows a waveform of a modulation voltage Vm applied from the data side electrode X. Figure 6 (2) shows the waveform of a writing voltage -Vm, +Vp applied from the scanning side electrode Y. Figure 6 (3) shows the waveform of a voltage applied to a picture element.

Appellants disclose on page 21 of the specification that as shown in Figure 6 (1), the pulse width of the modulation voltage VM for the first field of negative driving is determined by the graduation display data at the time of input to the data conversion circuit 18. Furthermore, Figure 6 (1)

shows that the pulse width of the modulation voltage Vm of the second field of positive drive is determined by inverting the graduation display data at the time of input to the data conversion circuit 18.

Appellants further disclose that the voltage waveform applied to the picture element as shown in Figure 6 (3) is determined by subtracting the modulation voltage waveform shown in Figure 6 (1) from the writing voltage waveform shown in Figure 6 (2). As shown in Figure 6 (3), the resulting voltage waveform applied to the picture element is a symmetrical voltage waveform.

The independent claim 1 is reproduced as follows:

1. A symmetrical drive method for driving a display device formed by interposing a dielectric layer between a plurality of scanning side electrodes and a plurality of data side electrodes whose intersections form a plurality of pixels, the symmetrical drive method comprising the steps of:

applying a positive writing voltage in one of a pair of fields, and applying a negative writing voltage in the other of the pair of fields, to each of the plurality of scanning side electrodes;

applying a first modulated voltage, to said plurality of pixels, with a time duration corresponding to a logical value of a binary code of a plurality of predetermined bits in said one of the pair of fields; and

inverting the logical value of the binary code of the plurality of predetermined bits to produce the binary complement of the logical value of the binary code of the plurality of predetermined bits and applying the binary complement as a second modulated voltage, to said plurality of pixels, in the other of the pair of fields, thereby providing a symmetrical voltage waveform to said plurality of pixels.

The Examiner relies on the following references:

Kanatani	4,488,150	Dec. 11, 1984
Flegal	4,733,228	Mar. 22, 1988
Inada	4,951,041	Aug. 21, 1990

Claims 1 and 3 through 5 stand rejected under 35 U.S.C. § 103 as being unpatentable over Inada in view of Kanatani and Flegal. Claims 2 and 6 through 9 stand rejected under 35 U.S.C. § 103 as being unpatentable over Inada in view of Kanatani.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs[2] and answers[3] for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 9 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed

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[2]Appellants filed an appeal brief on March 28, 1994. Appellants filed a reply appeal brief on August 15, 1994. The Examiner responded to this reply brief with a supplemental Examiner's answer on November 17, 1994, thereby entering and considering the reply brief. Appellants filed a supplemental reply appeal brief on January 13, 1995. The Examiner responded to this supplemental reply brief with a supplemental Examiner's answer on April 17, 1995, thereby entering and considering the reply brief. Appellants filed a reply appeal brief on June 19, 1995. The Examiner stated in the Examiner's letter dated February 15, 1996 that the June 19, 1995 reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

[3]The Examiner responded to the brief with an Examiner's answer, dated June 14, 1994. The Examiner responded to the August 15, 1994 reply brief with supplemental Examiner's answer dated November 17, 1994. The Examiner responded to the January 13, 1995 supplemental reply brief with a supplemental Examiner's answer dated April 17, 1995.

invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

In regard to the rejection of claims 1 and 3 through 5 under 35 U.S.C.§ 103 as being unpatentable over Inada in view of Kanatani and Flegal and the rejection of claims 2 and 6 through 9 under 35 U.S.C.§ 103 as being unpatentable over Inada in view of Kanatani, Appellants argue on pages 12 through 25 of the brief that Inada, Kanatani and Flegal, together or individually, fail to teach or suggest a symmetrical drive method which utilizes binary code signals and inverts the binary code signals in order to provide a

symmetrical voltage waveform as shown in Appellants' Figure 6. In particular, Appellants argue on pages 13 and 14 of the brief that as indicated in Figure 6 (1), the modulation voltage applied to the N driving field has a width W1 which corresponds to the claimed binary coded signal. Further, the

modulated voltage in the P driving field has a width W2 which corresponds to the binary complement of the width of the binary code signal W1 applied to the N driving field. Combining this modulation voltage with the writing voltage illustrated in Figure 6 (2) provides the symmetrical voltage waveform provided to the picture elements illustrated in Figure 6 (3). Appellants further argue that as is clearly illustrated in Figure 6 (3) the voltage waveform applied to the picture element in the N driving field is symmetrical to the voltage waveform applied to the picture element in the P driving field. As a result, Appellants argue that the Appellants' claims recite either a symmetrical drive method or apparatus that provides this symmetrical voltage waveform to the picture elements. Appellants argue on page 15 of the

brief that Inada does not teach the claimed symmetrical voltage because Inada teaches in Figure 4 that the waveform X2-Y1 has a voltage in the N frame that is not symmetrical to the voltage in the P frame.

Appellants reemphasize the point in all of the reply briefs. In particular, Appellants argue on page 4 of the June 19, 1995 reply brief that Figure 6 (3) illustrates a negative voltage being applied to a picture element and a positive voltage being applied to the same picture element. Appellants further argue

that if the first pulse in Figure 6 (3), namely the negative voltage pulse, is reoriented to a positive pulse, the first pulse is identical to the second pulse shown in Figure 6 (3).

Accordingly, Appellants submit that the waveform applied to the picture element in independent claims 1 through 9 is symmetrical, because a value represented by a binary coded signal is applied first to the picture element, and then the binary complement of the binary code signal is applied to the

picture element in order to obtain a symmetric voltage waveform as shown in Appellants' Figure 6 (3).

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." ***In re Hiniker Co.***, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). We note that Appellants' claim 1 recites "inverting the logical value of the binary code of the plurality of predetermined bits to produce the binary complement of the logical value of the binary code of the plurality of predetermined bits and applying the binary complement as a second modulated voltage, to said plurality of pixels, in other of the pair of fields, thereby providing a symmetrical voltage waveform to said plurality of pixels." Similarly, Appellants' claim 2

recites inverting the binary code signal so the gradation display data and its binary complement are utilized with the positive and negative writing voltage, respectively, to produce a symmetrical voltage waveform to the picture elements. We note that claims 2

through 6, 8 and 9 also recite similar language requiring the production of a symmetrical voltage waveform as shown in Figure 6 (3) which is then applied to the pixels. In reviewing claim 7, we note that Appellants claim "a data electrode driving circuit for applying a first modulated voltage with a time duration corresponding to a logical value of a binary code ... in a term corresponding to one electrode of the adjacent scanning side electrode pair, inverting the logical value of the binary code ... and for applying the binary complement as a second modulated voltage in a term corresponding to the other electrode of the adjacent scanning side electrode pairs, to the data side electrodes." Thus, claim 7 results in the production of a symmetrical voltage waveform as shown in Figure 6 (3) which is then applied to the pixels.

Upon a careful review of Inada, we find that the reference fails to teach the production of a symmetrical voltage waveform shown in Figure 6 (3) by inverting the binary code signal so the gradation display data and its binary complement are utilized

with the positive and negative writing voltage, respectively, to produce a symmetrical voltage waveform to the picture elements. Inada shows in Figure 4, waveforms X2-Y1 and X2-Y2 in which the positive and negative pulses are different when they are applied to the picture elements.

Furthermore, we fail to find any suggestion of modifying Inada to provide a symmetrical voltage waveform as recited in Appellants' claims 1 through 9. The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg.***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

We have not sustained the rejection of claims 1 through 9 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
PARSHOTAM S. LALL Administrative Patent Judge	)	

MRF/pgg

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