

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT P. COLWELL, ANDREW F. GLEW, ATIQ A. BAJWA,
GLENN J. HINTON and MICHAEL A. FETTERMAN

Appeal No. 96-2499
Application No. 08/204,521¹

ON BRIEF

Before KRASS, FLEMING and HECKER, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 3, 5 through 40 and 42 through 50. Claims 4 and 41 have been canceled.

¹ Application for patent filed February 28, 1994.

Appeal No. 96-2499
Application No. 08/204,521

The invention pertains to efficient processing performance within a superscalar microprocessor. More particularly, a method and apparatus are provided for allowing flag register renaming within a register alias table [RAT] and for proper updating of the flag bits upon retirement of operations that update flag bits.

Representative independent claim 16 is reproduced as follows:

16. A microprocessor comprising:

a bus interface unit for interfacing with an internal communication bus;

instruction decode and fetch unit coupled to said bus interface unit for decoding and supplying a current set of instructions within a common clock cycle wherein instructions of said current set of instructions read flag registers, said current set of instructions including a given instruction and a previous instruction wherein said previous instruction occurs previous to said given instruction in program code order;

an execution unit for executing instructions;

an architecturally visible register file comprising registers; and

register alias logic for renaming flag registers associated with said current set of instructions processed within said common clock cycle, said register alias logic comprising:

Appeal No. 96-2499
Application No. 08/204,521

(a) a memory array for providing a plurality of addressable entries for renaming said flag registers;

(b) array read logic coupled to said memory array and coupled to said logic for supplying, said instruction decode and fetch unit for addressing said memory array by said flag registers and for supplying pointers to a set of physical registers assigned to said flag registers;

(c) dependency logic for determining if said given instruction of said current set of instructions reads a flag register that is output by said previous instruction of said current set of instructions; and

(d) comparison logic responsive to said dependency logic for determining if flags of said flag register read by said given instruction are a superset of flags of said flag register output by said previous instruction of said current set of instructions.

The examiner relies on the following reference:

Cocke et al. (Cocke) 4,992,938 Feb. 12,
1991

Claims 1 through 3, 5 through 40 and 42 through 50 stand rejected under 35 U.S.C. § 103 as unpatentable over Cocke.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

Appeal No. 96-2499
Application No. 08/204,521

We will reverse the examiner's rejection of claims 1 through 3, 5 through 40 and 42 through 50 under 35 U.S.C. § 103.

Turning first to independent claim 16, which is representative of claims 8, 9, 15, 22 and 40, the examiner points to various portions of Cocke (pages 3-5 of the answer) as corresponding to the instant claimed invention. At page 5 of the answer, the examiner admits that Cocke does not explicitly teach the renaming of "flag registers," as claimed. However, the examiner concludes that it would have been obvious to apply Cocke's teachings to "flag registers" because Cocke teaches (column 3, lines 61-63) that "register renaming may be applied to any physical register set in the machine: GPR's, FPR's, status/control registers, etc." and that it "is well known" that status/control registers "are flag registers which contain a plurality of dynamically changeable flag bits and mask bits."

We agree that Cocke fails to teach the renaming of "flag registers," as claimed, but we disagree with the examiner that it would have been obvious, within the meaning of 35 U.S.C. § 103, to apply the teachings of Cocke to flag registers.

Appeal No. 96-2499
Application No. 08/204,521

As argued by appellants, at pages 28 et seq. of the brief, persuasively, in our view, the flag register of the instant claimed invention can be *partially* updated by any particular instruction. There is no partial updating of the status/control registers in Cocke, even if we assume, arguendo, that the status/control registers may be flag registers.

One might argue that the instant claim language of claim 16, for example, does not require the *partial* updating relied on by appellants. However, while the claim does not specifically recite a "partial updating," it is clear from the instant specification and the instant claim language that such partial updating is made possible by the claimed memory array which renames the flag register information output from each instruction to a physical register. Since the flag register may be partially updated, the flag register as output by a previous instruction may or may not provide the entire set of source flag information required for a subsequent instruction. This is the case when the given or subsequent instruction requires a "superset" of the flags of the flag register that

Appeal No. 96-2499
Application No. 08/204,521

are output by the previous instruction. The claimed "comparison logic..for determining if flags...read by said given instruction are a superset of flags of said flag register output by said previous instruction..." inherently allows for a partial updating because when a subsequent instruction requires a "superset" of the flags of the flag register that are output by the previous instruction, this can only arise when registers can be partially updated [see page 28 of the brief and page 87 of the specification]. As argued by appellants (page 29 of the brief), "[w]ithout the ability to allow partial register updating, the ordinary practitioner viewing Cocke's renaming system would have no motivation to check for 'superset' conditions, as claimed."

Moreover, we also agree with appellants that even if we assumed that the registers of Cocke can be partially updated, "Cocke provides absolutely no circuitry nor does Cocke provide any method by which to process the special conditions required to perform partial register updates" [brief-page 31].

Turning to claims 1 through 3 and 48, these claims also require the partial register updating capability discussed supra because they recite an array read means that supplies

Appeal No. 96-2499
Application No. 08/204,521

the physical register provided that "said logical source register does not require, as a source of data, a superset of said set of flag bits updated by said first instruction."

The examiner's counter (page 12 of the answer) that it is "old and well known" that the "status/control registers in any conventional computer system must have the ability to provide partial update by given instruction" is unconvincing since the examiner has offered no evidence of the fact he/she is relying on. Moreover, there is no evidence in Cocks of any particular means or method for performing such a partial register update. Further, the examiner contends that Cocks teaches a comparison means for "determining if an input tag for a given instruction is a superset of previous instruction" [answer-page 13] but the examiner is not very specific as to where such a teaching can be found in Cocks, pointing, very broadly, to columns "2-4, column 5...columns 9-15." Furthermore, the "tags" of Cocks appear to be no more than register names whereas the flags and flag registers of the instant claimed invention are control bits used to indicate the results of certain operations and processor conditions.

Appeal No. 96-2499
Application No. 08/204,521

Claims 5 through 7, 11 through 14, 18 through 21, 24 through 27, 43 and 50 will stand with the claims from which they depend. Accordingly, we also reverse the rejection of these claims under 35 U.S.C. § 103 as unpatentable over Cocke.

We turn to claims 28, 29, 32, 33, 36, 37 and 44. These claims recite both static and dynamic flag masks wherein *both* masks are used for updating flag bits when an instruction retires. We find absolutely no teaching or suggestion of the subject matter of these claims in Cocke. Apparently, neither does the examiner because, while admitting that Cocke fails to show the use of a static or dynamic flag (answer-page 10), the examiner finds that it would have been obvious to "implement a status/control register renaming system with static and dynamic flag masks...since [the reference] suggested that the register renaming can be applied to any type of registers...use of the static and dynamic flags is not a patentable distinction, but rather an engineering choice."

Clearly, the examiner has no basis for calling the static and dynamic flag masks "an engineering choice" since these masks are recited as having very specific functions and the examiner has pointed to nothing in the prior art exhibiting

Appeal No. 96-2499
Application No. 08/204,521

those functions. Further, there is no teaching in Cocke that the "status/control" registers are "flag registers," as claimed and now, the examiner is apparently contending not only that the recited status/control registers of Cocke are equivalent to the claimed flag registers but also that it would have been obvious to employ static and dynamic flag masks, as claimed. Clearly, the examiner is employing impermissible hindsight in constructing this rejection and we will not sustain such a rejection. Neither will we sustain the rejection of claims 30, 31, 34, 35, 38, 39 and 45 through 47 under 35 U.S.C. § 103 since these claims depend from claims 28, 32, 36 and 44.

Appeal No. 96-2499
Application No. 08/204,521

The examiner's decision is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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STUART N. HECKER)	
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Appeal No. 96-2499
Application No. 08/204,521

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