

# Ex parte Grochowski et al.

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

*Ex parte* EDWARD T. GROCHOWSKI  
and MUSTAFIZ R. CHOUDHURY

Appeal No. 96-2586  
Application 07/914,877<sup>1</sup>

ON BRIEF

MAILED

APR 1 - 1997

PAT. & T.M. OFFICE  
BOARD OF PATENT APPEALS  
AND INTERFERENCES

Before KRASS, JERRY SMITH and FLEMING, *Administrative Patent Judges*.

FLEMING, *Administrative Patent Judge*.

## DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 10 through 21. Claims 1 through 9 have been canceled. Appellants filed an after final amendment on March 10, 1995 canceling claims 10, 11, 14 and 15 and amending claims 12, 13 and 16 through 20. In the advisory action dated March 16, 1995, the Examiner stated that the March 10, 1995 amendment will be entered

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<sup>1</sup> Application for patent filed July 16, 1992.

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upon the filing of an appeal. We note that the record shows that the amendment is entered. Thus, claims 12, 13 and 16 through 21 are properly before us on appeal.

The invention relates to the field of microprocessor architecture. In particular, the invention relates to a cache memory having multiple address ports and corresponding multiple tag ports.

On page 1 of the specification, Appellants disclose that prior art microprocessor systems widely employ cache memories, both for storing data and for storing program instructions. In a multiprocessor environment, there is a need to insure that data or instructions modified in a cache of one processor are not used in another processor in unmodified form. In order to prevent this from occurring, it is conventional to "snoop" in each cache to determine if a particular line is present when such line is being modified. If the line is found, the state of that cache line is modified in accordance with a cache coherency protocol implemented by the system. Because the prior art caches are single ported, snooping generally exacts a performance penalty. Appellants disclose on page 2 of the specification, that their invention addresses this problem by providing a cache in which snooping for one address can be conducted concurrently with one or more references to different addresses in a single clock cycle.

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On page 5 of the specification, Appellants disclose that the invention is embodied in a P5 microprocessor. The P5 is a superscalar microprocessor having dual instruction pipelines. On page 6 of the specification, Appellants disclose that the porting of the data cache is illustrated in Figure 1. Microprocessor 110 includes two pipelines, u pipe 100 and v pipe 101. The Data cache 10 has three address ports 11, 12 and 13 which are dedicated to snooping, the u-pipe 100 and the v-pipe 101, respectively. On page 7, Appellants disclose that Tag ports 14, 15 and 16 are associated also with the three address ports 11, 12 and 13 respectively. Data cache 10 is provided with a single data port 17.

On page 7 of the specification, Appellants refer to Figure 2 and disclose that the code cache 20 has address ports 21, 22 and 23. Address port 21 is dedicated to snooping whereas ports 22 and 23 accommodate split-line accesses in support of branch cycles to the upper half of a cache line. Thus, the code cache is capable of retrieving the upper half of that line and the lower half of the next line, all in the same clock cycle.

Independent claims 13 and 16 are reproduced as follows:

13. An instruction cache for processing branch instructions comprising:

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a plurality of lines of the cache, each line comprising a plurality of banks of data, each line having an associated tag and each bank identified by an associated memory location address;

first and second address ports for concurrently providing a first memory location address and second memory location address;

first and second tag ports respectively associated with the first and second address ports for concurrently providing tag data to the cache corresponding respectively to the first and second memory location addresses; and

a single data port for providing data located at the memory location addresses provided at the first and second address ports, the bandwidth of the single data port being sufficient to accommodate a plurality of predetermined sized banks, a location of each of said plurality of banks provided to the single data port identified by the memory location address and second memory location address respectively provided at the first and second address ports; wherein if a branch instruction is executed causing a first memory location address to be input to the first address port and a second memory location address to be input to the second address port, said first memory location address identifying a last bank of a first cache line and the second memory location address identifying a first bank in a second cache line, said cache providing data of said first and second banks concurrently to the data port.

16. A microprocessor system comprising:

a first pipeline for execution of instructions;

a second pipeline for execution of instructions;

a cache comprising a plurality of bits of information organized into lines, each line having an associated tag and a plurality of associated memory location addresses identifying associated memory locations on each line of the cache, said cache comprising a first address port coupled to the first pipeline for receiving first memory location addresses and a second address port coupled to the second pipeline for concurrently receiving second memory location addresses, and first and second tag ports respectively coupled to the first and second pipelines and associated with the first and second address ports for

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concurrently receiving tag data to the cache corresponding respectively to the first and second memory location addresses, and a single data port coupled to the first and second pipelines for providing data located at the memory location addresses provided at the first and second-address ports.

The Examiner relies on the following references:

Inagami et al. (Inagami)	4,782,441	Nov. 1, 1988
Ikumi	5,228,135	Jul. 13, 1993
		(filed Jan. 25, 1991)

Claims 12, 13 and 16 through 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ikumi and Inagami<sup>2</sup>.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief<sup>3</sup> and answer for the respective details thereof.

#### OPINION

We will not sustain the rejection of claims 12, 13 and 16 through 21 under 35 U.S.C. § 103.

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<sup>2</sup> In the March 16, 1995 advisory action, the Examiner states that the Applicants' response has overcome the 35 U.S.C. § 112 rejections. On page 4 of the answer, the Examiner withdraws the rejection of claims 12, 18 and 19 under 35 U.S.C. § 103 as being unpatentable over Suzuki or Watanabe.

<sup>3</sup> Appellants filed an appeal brief on July 6, 1995. We will refer to this appeal brief as simply the brief. Appellants filed a reply brief on December 28, 1995. The Examiner stated in the Examiner's letter dated January 16, 1996 that the reply brief has not been entered.

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The Examiner argues that all of the claims stand or fall together. We note that Appellants do state that claims 12, 13 and 16 through 21 stand or fall together on page 4 of the brief. However, we also note on pages 4 and 5 of the brief, that Appellants' have argued claims 13 and 16 separately and have explained why claims 13 and 16 are believed to be separately patentable over the applied art. In accordance with 37 CFR § 1.192(c)(7), revised as of July 1, 1995 that "[f]or each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of the claim alone unless ... in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable." We find that claims 12 and 13 as one group stand or fall together with claim 13 as the selected claim of that group for decision on appeal and claims 16 through 21 as another group stand or fall together with claim 16 as the selected claim of that group for decision on appeal.

The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained

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in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), citing *W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Appellants state that claim 13 is directed to an instruction cache which accommodates split line accesses in support of branch cycles. Appellants state that at the top of page 8 of the specification, the specification discloses that the upper half of one line is retrieved and the lower half of the next line is retrieved in which both are provided in the same clock cycle. Appellants argue that neither reference teaches or suggests the execution of a branch instruction "causing a first memory location address to be input to the first address port and a second memory location address to be input to the second address port, said first memory location address identifying a last bank of a first cache line and the second memory location address identifying a first bank in a second cache line, the cache providing data of the first and second banks concurrently to the data port" as recited in Appellants' claim 13.

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The Examiner does not provide any showing in either Ikumi or Inagami of the above limitation. The Examiner addresses this issue on page 4 of the answer. The Examiner argues that it would have been obvious "that branch instructions can be performed by a CPU, and different lines could access the invention realized by the combination of teachings of Ikumi and Inagami et al., providing a faster and more efficient system." On page 5 of the answer, the Examiner states that it "is well within the scope of the teaching of the combination of Ikumi and Inagami et al. that branch instructions can be performed by a pipelined ALU, which would result in the access of any combination of lines in the multi-port cache memory." However, the Examiner provides no evidence in the prior art to support this legal conclusion.

We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a *prima facie* case. *In re Knapp-Monarch Co.*, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961). *In re Cofer*, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Therefore, we will not sustain the Examiner's rejection of claims 12 and 13 under 35 U.S.C. § 103.

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On page 5 of the brief, Appellants argue that the combination of Ikumi and Inagami would not have led those skilled in the art to provide a pipeline processor with separate address ports for each pipe as set forth in Appellants' claim 16. We note that Appellants' claim 16 recites a "cache comprising a first address port coupled to the first pipeline for receiving first memory location addresses and a second address port coupled to the second pipeline for concurrently receiving second memory location addresses, and first and second tag ports respectively coupled to the first and second pipelines and associated with the first and second address ports for concurrently receiving tag data to the cache corresponding respectively to the first and second memory location addresses, and a single data port coupled to the first and second pipelines for providing data located at the memory location addresses provide at the first and second address ports."

On a closer reading, it is revealed that Inagami teaches a vector processor which executes a plurality of instructions in which a large amount of data is processed. In column 2, lines 15-43, Inagami teaches that Figure 1 shows a configuration of a vector processor in accordance with Inagami's invention. Inagami teaches that each of the pipelined ALUs 3-1 and 3-2 accesses a

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main storage 1 via address registers 6. Thus, Inagami does not contemplate having each pipeline access the main storage via a separate address port.

The Examiner argues on page 3 of the answer that it would have been obvious to one having ordinary skill in the art to have utilized pipelined ALUs, as taught by Inagami in the Ikumi system. However, this does not address a number of Appellants' claimed limitations as recited in Appellants' claim 16. First, the Examiner has not addressed how Inagami or Ikumi teaches or suggests having a first address port coupled to the first pipeline for receiving first memory location addresses and a second address port coupled to the second pipeline for concurrently receiving second memory location addresses. Secondly, the Examiner has not addressed how Inagami or Ikumi teaches or suggests having the first and second tag ports respectively coupled to the first and second pipelines and associated with the first and second address ports for concurrently receiving tag data to the cache corresponding respectively to the first and second memory location addresses. Finally, the Examiner has not addressed how Inagami or Ikumi teaches or suggests a single data port coupled to the first and

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second pipelines for providing data located at the memory locations addresses provided at the first and second address ports.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), *citing In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." *Para-Ordnance Mfg. v. SGS Importers Int'l*, 73 F.3d at 1087, 37 USPQ2d at 1239, *citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

We agree that if there were a teaching to combine Ikumi and Inagami, one of ordinary skill in the art would have been led to modify the Ikumi multiple processor system by having at least one Inagami pipeline processor wherein the Inagami processor accesses the cache through the same address port. We fail to find any suggestion in either Ikumi or Inagami to provide a pipeline processor with separate address ports for each pipe of the pipeline processor as recited in Appellants' claim 16.



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