

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DONALD E. CARMON

Appeal No. 96-3085
Application 08/274,655¹

ON BRIEF

Before JERRY SMITH, FLEMING and LALL, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims claims 1 through 4, and 8 through 11. Claims 5 through 7 have

¹ Application for patent filed July 13, 1994. According to appellant, the application is a continuation of Application 07/766,490, filed September 26, 1991, now abandoned.

been cancelled².

The disclosed invention relates to a method and apparatus for counting and monitoring processor execution cycles associated with a specific task running concurrently with other tasks in a hard real-time, multi-tasking microprocessor such as a single processor. Such a processor runs multiple tasks by dividing its execution cycles up among the specific tasks. The invention provides that each task has a specific processor cycle count allocated to it initially. A counter is loaded with this allocated count initially. The method and apparatus of the invention decrement a counter for a specific task only when an execution cycle is allocated to perform that specific task. When a specific task reaches its allocation, an appropriate cycle counter interrupt is generated.

Representative claim 1 is reproduced as follows:

1. In a multi-tasking program execution system, a method of monitoring task overrun conditions, the method comprising the steps of:

counting only processor execution cycles associated with a specific task occurring while said specific task is executed, said specific task being executed together with one or more

² No amendments after the final rejection were filed.

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other tasks by a single processor; and

generating a cycle counter interrupt which is one type of processor execution interrupt whenever said counting reaches a predetermined value; and

stopping said counting whenever any processor execution interrupt occurs.

The references relied on by the examiner are:

Bogaert et al.(Bogaert)	4,432,051	Feb. 14, 1984
Peet, Jr. et al.(Peet)	5,146,589	Sept. 8, 1992

Claims 1 through 4 and 8 through 11 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the Examiner offers Bogaert and Peet [answer, page 3].

Reference is made to Appellant's brief and the Examiner's answer for their respective positions.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1 through 4 and 8 through 11.

With respect to independent claim 1, the Examiner basically takes the position that Peet shows everything except

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that it does not explicitly detail the step of simultaneously counting execution cycles associated with a specific task being executed together with one or more other tasks by a single processor (a multi-tasking processor). The Examiner asserts that it would have been obvious, to one of ordinary skill in the art at the time of the invention, to modify the teachings of Peet to yield a system as claimed by using a single processor instead of multiple processors to track a specific task and any other tasks

associated thereto[,] because said modification would [have] reduce[d] the amount of processors necessary to track a plurality of tasks including a specific one [final rejection, page 3].

Appellants argue that the invention establishes a counter with a count for each specific task running concurrently with other tasks in a single processor. The invention counts only cycles associated with a specific task even if other tasks are running concurrently. Counting is suspended for interrupts, even though the handling of an interrupt uses

processor execution cycles [brief, page 6].

The examiner responds that Peet discloses a counter that counts machine cycles in the synchronization process of the CPU's, said counter is stopped when it reaches a maximum value, which indicates that the CPU's are in synchronization [answer, page 5]. The Examiner cites column 9, line 65 to column 10, line 17 of Peet which state that: " A cycle counter 71 is coupled to the clock 17 ... to count machine cycles which are Run cycles (but not Stall cycles). This counter 71 includes a count register having a maximum count value selected to represent the period during which the maximum allowable drift between CPU's would occur ...; when this count register overflows [, an]action is initiated to stall the faster processors [until slower

processor or processors catch up]. This counter 71 is reset whenever synchronization is done ... circuit 65." The Examiner concludes that the counter of Peet does stop counting, and the step[s] of counting processor execution cycles associated with a specific task, and [of] generating a

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cycle counter interrupt[,] called for by claim 1[,] are clearly taught by Peet [answer, pages 5 and 6].

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (CCPA 1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.,

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776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

As indicated by the cases just cited, the Examiner has at least two responsibilities in setting forth a rejection under 35 U.S.C. § 103. First, the Examiner must identify all the differences between the claimed invention and the teachings of the prior art. Second, the Examiner must explain why the identified differences would have been the result of an obvious modification of the prior art.

In our view, the Examiner has addressed his first responsibility, but has not met his second responsibility.

We agree with Appellant that Peet, the sole reference used in rejecting this claim, does not meet the limitations called for in claim 1. Peet relates to a multiple-processors system where the same stream of instructions is being executed by three identical CPU's [column 2, line 30 to column 3, line

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68]. The objective is to run these three CPU's in
synchronization to

assure redundancy. Whenever they are out of synchronization
in a machine cycle, the counter register 71, which is
preloaded with a maximum allowable drift count value, is
decremented by one. When the counter reaches the maximum
allowable drift value, the processing in the faster CPU or
CPU's is stalled, synchronization among the CPU's is obtained,
and the counter is reset. Thus, there is an interrupt signal
when the counter reaches a predetermined value.

However, the counting done by the counter of the
invention is different from that done by counter 71 of Peet.
Peet's counter counts all the machine cycles continuously as
the CPU's are processing incoming instructions, which might
include interrupts, whereas the Appellant's counter counts
only those machine cycles which are exclusively ascribed to a
specific task, out of the many other multiple tasks, and all
the multiple tasks are being executed by a single CPU. Thus,
if an interrupt occurs due to the need to service another

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specific task of higher priority, then Appellant's counter associated with the prior specific task would stop counting. There is no such provision in Peet. Peet's counter 71, on the other hand, keeps on counting as long as the maximum drift value is not reached.

Thus, we are unable to see how Peet's system can be modified to meet the feature of "counting only processor execution cycles associated with a specific task occurring while said specific task is executed, said specific task being executed together with one or more other tasks by a single processor;..." [claim 1, lines 4 through 7].

Therefore, we reverse the rejection of claim 1.

As to the rejections of claims 2, 4/1, 4/2 and 8 through 11, which are all rejected under 35 U.S.C. § 103 as being obvious over Peet, they are reversed for the same rationale. They all contain, among others, the feature discussed above, in the form of method or apparatus.

With regard to claims 3/1 and 3/2, the Examiner has

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rejected these claims under 35 U.S.C. § 103 as being unpatentable over Peet in view of Bogaert. Bogaert relates to a time accounting system for accounting for the time a process spends in a ready state, a wait state, or a running state. Bogaert does not cure the above noted deficiency of Peet. Therefore, we reverse these obviousness rejections of claims 3/1 and 3/2.

In conclusion, we reverse the rejections of claims 1, 2, 4/1, 4/2 and 8 through 11 under 35 U.S.C. § 103 as being

unpatentable over Peet, and the rejections of claims 3/1 and 3/1 under 35 U.S.C. § 103 as being unpatentable over Peet in view of Bogaert.

DECISION

The decision of the examiner rejecting claims 1 through 4 and 8 through 11 under 35 U.S.C. § 103 is reversed.

REVERSED

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