

**THIS OPINION WAS NOT WRITTEN FOR PUBLICATION**

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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**Ex parte** JEFFREY I. ROBINSON  
and KEITH ROUSE

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Appeal No. 1996-3708  
Application 07/474,742

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ON BRIEF

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Before HAIRSTON, JERRY SMITH, and FLEMING, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

**DECISION ON APPEAL**

This is a decision on appeal from the final rejection of claims 1 through 13, 15 through 34 and 36 through 38. Claims 14 and 35 have been canceled.

The invention relates to an apparatus the architecture of which permits the instantaneous realization of certain classes of system in integrated circuit or discrete circuit form. On pages 6 through 7 of the specification, Appellants disclose that figure 1 shows a block diagram of the invention. The apparatus includes a plurality of functional blocks 20 and a central core. The communication between the blocks is via core 30. The core is the physical heart of the apparatus and is responsible for interfacing with main communications bus 40. The core interprets all data into and out of the apparatus, including parametric, microcode and topological data, and provides data routing via a non-blocking matrix switch.

Independent claim 1 is illustrative of the invention.

1. A programmable apparatus for interfacing with a communications bus, said apparatus comprising:

a) a plurality of programmable signal processor means having means for receiving and storing parameters and microinstructions, and means for executing microinstructions, each said programmable signal processor means for performing an operation according to said microinstructions and said parameters on signal data received by said programmable signal processor means;

b) a core means comprising interface means for interfacing with said communications bus, decoder means for distinguishing between at least topological and parametric data received by said core means over said communication bus,

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and matrix switching

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means for interconnecting at least two of said plurality of programmable signal processor means in a desired manner in response to said topological data received over said communications bus;

c) a plurality of data bus means for connecting said plurality of programmable signal processor means to said matrix switching means; and

d) at least one third bus means coupled to said core means and to said means for receiving and storing, for transmitting parametric data and said microinstructions to said means for receiving and storing of at least a plurality of said programmable signal processor means.

The Examiner relies upon the following reference:

Engels et al. (Engels), "Concept and Implementation of a Powerful Multiprocessor System for Digital Signal Processing," January 4, 1989.

Claims 1 through 13, 15 through 34 and 36 through 38 stand rejected under 35 U.S.C. § 102 or in the alternative under 35 U.S.C. § 103 as being unpatentable over Engels.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs<sup>1</sup> and answer for the respective details thereof.

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<sup>1</sup>Appellants filed an appeal brief on February 15, 1996. Appellants filed a reply brief on August 1, 1996. On August 20, 1996, the Examiner mailed a communication stating that the reply brief has been entered and considered.

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### OPINION

We will not sustain the rejection of claims 1 through 13, 15 through 34 and 36 through 38 under either 35 U.S.C. §§ 102 or 103.

#### **The 35 U.S.C. § 102 Rejection**

First we will consider the rejection of the claims under 35 U.S.C. § 102 as being anticipated by Engels. Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Applied Digital Data Sys. Inc.*, 730 F.2d 1440, 1444, 221 USPQ 385,388 (Fed Cir. 1984), **cert.** dismissed, 468 U.S. 1228 (1984); *W. L. Gore & Assocs., Inc. v. Garlock Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), **cert. denied**, 469 U.S. 851 (1984).

The Examiner states on page 7 of the answer that the claimed programmable signal processors are met by Engels' DSPs in figure 2. The Examiner further states on page 7 of the brief that the claimed third (parametric) bus means connecting

the core with the processors (Engels DSPs) is met by the data bus on the left side of Engels figure 1. On page 6 of the answer, the Examiner states that the core's decoder is met by Engels HOST (Figure 1). The Examiner further states on page 7 of the answer that the claimed matrix switch of the core is met by the LCAs of figure 2. On pages 7 and 8 of the answer, the Examiner admits that Engels does not explicitly teach the claimed communications bus, but asserts that "it would have been self-evident/logical that Engels' system provided for such a network/bus interface to other processors." The Examiner supports this assertion by citing section 4.3 of Engels which identifies that a bus (apparently the bus identified in figure 1 with three lines labeled Address, Data and Control) will connect the HOST and the DSP to I/O devices which will allow other computers to be connected.

On page 15 of the appeal brief, Appellants argue that the claimed function of the core differs from the Engels' device. Appellants assert on page 17 of the brief that the claims recite a core means comprising interface means for interfacing with the communication bus, decoder means for distinguishing between topological and parametric data and matrix switching

means. On pages 16 and 17 of the appeal brief, Appellants argue that interpreting the processor of the host as the claimed decoder means and the LCAs as the claimed matrix switching means does not meet the claims as these means are not both in the core. Similarly interpreting the Engels bus controller as the claimed bus interface means does not meet the claim as the Engels bus controller is not in a core with the encoder and switching matrix.

We find that the scope of all of the independent claims, except claim 18, includes a device having a communications bus and a central core. The core contains a communication bus interface, a decoder and a switching matrix. These limitations are found in exemplary claim 1 "b) a core means comprising interface means for interfacing with said communications bus, decoder means for distinguishing between at least topological and parametric data received by said core means over said communications bus, and matrix switching means. . . ." Virtually identical limitations are found in independent claims 7, 15, 20, 29, 36. Similarly the scope of claims 17 and 38 is found to include a communications bus and

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a core which contains an interface with the communications bus  
and the matrix switching means (claim 17 "a core means capable  
of interfacing with said communications bus and of  
interconnecting at least two of said

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plurality of programmable signal processors means in a desired manner") and the decoder (claim 17 ". . . and at least one third bus means for obtaining and carrying parametric data . . . ." ).

We find that the Examiner has failed to show that each limitation of the claims is anticipated by the prior art. In particular the Examiner has not shown that Engels discloses a communications bus or a central core which contains an interface with the communications bus, an encoder and switching matrix. We find that Engels teaches that the HOST generates data and transmits it to the DSP boards. Furthermore, we find that Engels discloses that the LCAs perform the switching matrix function. We find that Engels fails to disclose Appellants' claimed core which provides all three functions of interfacing, decoding and switching. Thus, we will not sustain the Examiner's rejection of claims 1 through 13, 15 through 17, 20 through 34 and 36 through 38 under 35 U.S.C. § 102.

We next consider the 35 U.S.C. § 102 rejection of claims 18 and 19. We find that the scope of independent claim 18, includes a communications bus and core containing an interface

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with the communications bus, a decoder and two additional buses to transmit the decoded data from the core to the signal processor.

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We find that the Examiner has failed to show that each limitation of the claims is anticipated by the prior art. In particular the Examiner has not shown that Engels discloses a communications bus or a central core which contains an interface with the communications bus, and an encoder. We find that the Engels reference discloses a HOST which generates data and transmits it to boards which contain several DSPs. Further we find that each DSP individually interfaces with the host. We find that the Engels reference fails to disclose a core which interfaces with a communications bus, decodes data received from the communications bus and transmits the data to the signal processor. We find that Engels fails to disclose Appellants' claimed core which provides all three functions of interfacing, decoding and transmitting. Thus, we will not sustain the Examiner's rejection of claims 18 and 19 under 35 U.S.C. § 102.

#### **The 35 U.S.C. § 103 Rejection**

Next we consider the rejection of the claims under 35 U.S.C. § 103 as being obvious over Engels in view of the

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knowledge of one of ordinary skill in the art. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings of suggestions found in the prior art, or by the implication contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention. " ***Par-Ordance Mfg. V SGS Importers Int'l Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995)(***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984)).

As stated above, the Examiner has not shown that Engels discloses a communications bus or a central core which contains an interface with the communications bus, a switching matrix and an encoder. On pages 7 and 8 of the answer the Examiner admits that Engels does not explicitly teach the claimed communications bus, but asserts that "it would have been self-evident/logical that Engels' system provided for

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such a network/ bus interface to other processors." The Examiner states "the concept of using dedicated computer-aided-design (CAD) machines to act as servers for clients located at many sites on a network was well-known at

the time of Appellants' invention." The Examiner argues that with this knowledge one of ordinary skill in the art reading Engels would have recognized that the data for the circuit configuration could be submitted to the HOST from a network. The Examiner asserts that in such a combination the data connection to the network would meet the claimed communications bus. The Examiner has not directly addressed the limitations of a core containing a decoder, an interface with the bus and a switching matrix. However, the Examiner asserts that one with the knowledge of ordinary skill in the art would have interpreted Engels to read on the claimed device.

On page 15 of the appeal brief, Appellants argue that the claimed function of the core differs from Engels' device. Appellants assert on page 17 of the brief that the claims call

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for a core means comprising, interface means for interfacing with the communications bus, decoder means for distinguishing between topological and parametric data and matrix switching means. On pages 16 and 17 of the appeal brief, Appellants argue that interpreting the processor of the host as the claimed decoder means and the LCAs as the claimed matrix switching means does not meet the claims as these means are not both in the core. Similarly interpreting the Engels bus controller as the claimed bus interface means does not meet the claim as Engels' bus controller is not in a core with the encoder and switching matrix.

We find that the Examiner has failed to present a **prima facie** case of obviousness in the rejection of claims 1 through 13, 15 through 17, 20 through 34 and 36 through 38. As addressed above we find that the scope of the independent claims includes a device having a communications bus and a central core. The core contains a communication bus interface, a decoder and a switching matrix. We find that the Examiner has failed to show that each limitation of the claims is taught in the prior art. We find that Engels fails to

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disclose Appellants' claimed communications bus or a core which provides all three functions of interfacing, decoding and switching. Further, we find that the Examiner has not shown that the prior art suggests any reason to modify Engels to provide a communications bus or a central core which contains an interface with the communications bus, an encoder and switching matrix.

We next consider the 35 U.S.C. § 103 rejection of claims 18 and 19. We find that the Examiner has failed to present a **prima facie** case of obviousness. As identified above we find the scope of independent claim 18 includes a communications bus and core containing an interface with the communication bus, a decoder and two additional buses to transmit the decoded data from the core to the signal processor. We find that the Examiner has failed to show that each limitation of the claims is taught in the prior art. We find that Engels fails to disclose a core which interfaces with a communications bus, decodes data received from the communications bus and transmits the data to the signal processor. Further, we find that Examiner has not shown that

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the prior art suggests any reason to modify Engels to provide a communications bus or a central core which contains an interface with the communications bus, and an encoder.

The Examiner's assertion in the 35 U.S.C. § 103 rejections that computer networks are well known in the art, therefore replacing the host with a network would provide the claimed communication bus, is unsupported by evidence in the record. We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a **prima facie** case. *In re Piasecki*, 745 F.2d 1468, 1471-72, 233 USPQ 785, 787-88 (Fed. Cir. 1984); *In re Knapp-Monarch Co.*, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); *In re Cofer*, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Furthermore, our reviewing court states in *In re Piasecki*, 745 F.2d at 1472, 223 USPQ at 788, the following:

The Supreme Court in *Graham v. John Deere Co.*, 383 U.S. 1 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under Section 103. As adapted to ex parte procedure,

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Graham is interpreted as continuing to place the "burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under section 102 and 103". **Citing *In re Warner***, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967).

As there is no evidence to support the assertion of the secondary teaching we will not sustain the rejection of claims 1 through 13, 15 through 34 and 36 through 38 under 35 U.S.C. § 103.

#### **The Issue of whether Engels is Prior Art**

On page 28 of the appeal brief, Appellants argue that the Engels reference is not prior art under § 102 as it is published after the filing date of the parent application.<sup>2</sup> Appellants assert it is improper for two reasons a) the publication date

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<sup>2</sup> This application is a continuation in part of application 07/217,616 filed on July 11, 1988, now U.S. Patent 5,068,823, the earliest of dates identified on the Engels reference is December 1988.

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cannot be readily ascertained and b) that Examiner should be estopped from denying the priority date of the parent application as the Examiner made a determination that the differences between the parent and the present application are obvious. Appellants Note that an obvious type double patenting rejection has been applied based upon the parent, U.S. Patent 5,068,823, in which the Examiner determined that the difference between the parent case and the subject case were obvious. Appellants overcame the double patenting rejection by filing a terminal disclaimer. Appellants assert on page 32 of the appeal brief that if the disclosure of the parent application itself is sufficient to support the claims then the CIP application should be entitled to the parent's filing date.

On page 25 of the answer, the Examiner provided reference to other documents which identify the publication date of the Engels article as January 4, 1989 and asserts that the date identified on the face of the document is erroneous. With regard to Appellants second point, the Examiner states on page 26 of the answer that the present application is a continuation-in-part application for the purpose of

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introducing new matter. From this argument the Examiner concludes that Appellants' application is not entitled to the prior filing date.

In view of our finding that Engels fails to teach or suggest Appellants' claimed invention, we do not need to reach this issue and find the issue moot<sup>3</sup>.

In view of the forgoing we will not sustain the rejection of claims 1 through 13, 15 through 34 and 36 through 38 under

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<sup>3</sup> However, even if we were to reach this issue we would not have been able to make the determination. The Examiner has not provided the necessary findings to establish that the application is not entitled to the parent application's filing date. Our reviewing court set forth the proper legal analysis to determine whether a later filed CIP is entitled to the benefit of the parent application's filing date. In ***Paperless Accounting Inc. v. Bay Area Rapid Transit System***, 804 F.2d 659, 663-64, 231 USPQ 649, 652 (Fed. Cir. 1986) "[T]he mere filing of a continuation-in-part with additional matter or revised claims is not itself an admission that the matter is 'new' or that the original application was legally insufficient to support the claims" (citing ***State Industries, Inc. v. A.O. Smith Corp.***, 751 F.2d 1226, 1233, 224 USPQ 418, 422 (Fed Cir. 1985)). The proper legal analysis requires the determination of whether the added matter was known and available to the public at the time of filing of the parent application. ***Id.*** at 664, 231 USPQ at 653. This is a determination that the Examiner must make before we can provide a ruling. In addition, matters are further complicated by the Examiner's rejection of the claims under obviousness type double patenting.

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either 35 U.S.C. §§ 102 or 103. Therefore, the decision of the Examiner rejecting claims 1 through 13, 15 through 34 and 36 through 38 is reversed.

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**REVERSED**

KENNETH W. HAIRSTON	)	
Administrative Patent Judge)	)	
)	)	
)	)	BOARD OF PATENT
JERRY SMITH	)	APPEALS AND
Administrative Patent Judge)	)	INTERFERENCES
)	)	
)	)	
MICHAEL R. FLEMING	)	
Administrative Patent Judge)	)	

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