

The opinion in support of the decision being entered today (1) was **not** written for publication in a law journal and (2) is **not** binding precedent of the Board.

Paper No. 58

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHIGEYOSHI WATANABE, TSUNEAKI FUSE,
KOJI SAKUI, MASAKO OHTA, YUKIHITO OOWAKI,
KENJI NUMATA and FUJIO MASUOKA

Appeal No. 1996-3846
Application No. 08/251,649

ON BRIEF

Before JERRY SMITH, BARRETT, and DIXON, **Administrative Patent Judges**.
DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 and 37. Claims 24-36 also remain in this application, but issues thereto have been addressed in a separate decision mailed March 14, 2000.

We REVERSE.

BACKGROUND

The appellants' invention relates to a dynamic random access memory (RAM) device which uses a high impedance buffer circuit interposed between the BIMOS differential amplifier and the bit-line pair. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A dynamic semiconductor memory comprising:

parallel word lines provided on a substrate;

parallel bit lines provided on the substrate to insulatively cross with said word lines, said bit lines including a bit-line pair having a first bit line and a second bit line;

memory cells connected to crossing points of said word lines and said bit lines, said memory cells comprising voltage controlled unipolar transistors and capacitors; and

sense amplifier means connected to said bit-line pair, for sensing and amplifying a difference between potentials on said first and second bit lines when a memory cell connected to said bit-line pair is selected from among the memory cells in a data readout mode, said sense amplifier means comprising a BIMOS differential amplifier circuit having a voltage-controlled unipolar transistor and current-controlled bipolar transistors functioning as driver elements and each of which have a base electrode;

said sense amplifier means further comprising a CMOS current mirror circuit connected to said first and second bit lines and said base electrodes of said current-controlled bipolar transistors.

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The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Miyamoto	4,616,342	Oct. 7, 1986
Ogiue et al. (Ogiue)	4,713,796	Dec. 15, 1987
Watanabe et al.(Watanabe) ¹	JP 61-142594	Jun. 30, 1986

Claim 1 stands rejected under 35 U.S.C. § 103 as being unpatentable over Ogiue in view of Miyamoto. Claim 37 stands rejected under 35 U.S.C. § 102(a) as being anticipated by Watanabe.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 39, mailed Dec. 19, 1995), and supplemental examiner's answer (Paper No. 54, mailed Jun. 28, 2000) for the examiner's reasoning in support of the rejections, and to the appellants' brief (Paper No. 38, filed Jul. 24, 1995), reply brief (Paper No. 42, filed Feb. 20, 1996) and supplemental reply brief (Paper No. 55, filed Aug. 28, 2000) for the appellants' arguments thereagainst.

¹ Translation by Schreiber Translations, Inc. Feb. 2000. All citations to Watanabe are to this translation

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

The examiner maintains that Ogiue discloses a current mirror that is connected indirectly to bit lines and base electrodes of the bipolar transistors. (See supplemental answer at page 2.) Appellants argue that Figure 12 of Ogiue shows that the current mirror (T35, T36, T38) is connected to the bipolar transistors and is not connected to the first and second bit lines and the base electrodes of the current-controlled bipolar transistors. (See reply brief at page 1.) We agree with appellants. Appellants argue that Miyamoto similarly shows in Figure 4 that the current mirror (53-56) is connected to the bipolar transistors (38, 39) and is not connected to the first and second bit lines and the base electrodes of the current-controlled bipolar transistors. (See reply brief at pages 1-2.) We agree with appellants. Moreover, the examiner has not provided a convincing line of reasoning why it would have been obvious to one of ordinary skill in the art at the time of the invention to connect the "sense amplifier means further comprising a CMOS current mirror circuit connected to said first and second bit lines and said base electrodes of said current-controlled bipolar transistors" as recited in the language of claim 1. Since the examiner

has not shown a teaching or provided a convincing line of reasoning to meet the limitations of claim 1, we cannot sustain the rejection of claim 1.

With respect to claim 37, the examiner maintains that “Watanabe in figures 5 and 8 discloses a first pair (Q1, /Q1) [sic, D1, /D1] and second pair (Q3, /Q3) [sic, D3, /D3] of bit lines, sense amplifiers (SA3) and (SA2) which selectively (using signals [blank], [blank]) [to] prevent communication between output lines.” (See supplemental answer at page 2.) This is a slightly different position than the examiner originally maintained in the answer at page 4. There the examiner stated “[s]ee Figure 8 with bit lines pairs connected to differential amplifiers SA2 whose outputs are connected in common to first and second output lines and bipolar transistors for preventing communication.” With the original statement of the rejection, it appears that the examiner relies upon two sense amplifiers SA2 and using pairs of data lines D1 and D2. With this basis as the rejection, the Appendices A and B attached to the reply brief would appear to be correct and communication would not be prevented. The examiner has not contradicted appellants’ analysis beyond a statement that “it is not possible to selectively prevent communication between first and second output lines.” (See supplemental answer at page 3.) This assertion by the examiner does not address the teaching or lack of teaching of Watanabe relative to the claimed invention. Here, the issue is not enablement or particularity of the claimed invention, but whether Watanabe anticipated the invention as recited in claim 37.

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Here, we agree with appellants that Watanabe does not anticipate the invention as recited in claim 37 based upon the examiner's original rejection as recited in the answer.

Appellants argue that Watanabe does not teach or suggest "selectively preventing communication (leakage current) between the output lines of the buffer differential amplifiers" as recited in claim 37. (See brief at page 8.) Appellants argue that the leakage paths shown in Appendices A and B attached to the Reply brief show the appropriate leakage path for communication. We agree with appellants. From our review of Watanabe and the examiner's correlation of the disclosed elements to the claimed invention at page 2 of the supplemental answer, we find that the examiner's correlation is not tenable to the invention as claimed. In the supplemental answer, the examiner relies upon (SA3), (SA2) along with data lines D1 and D3 to achieve the common connection of the outputs. With this statement of the rejection, the combination of the SA2, level shifter and SA3 would have to be equated to the claimed buffer differential amplifiers, but the examiner has not set forth this in the rejection, leaving us to speculate as to the proper application of the prior art to the claimed invention. Moreover, if SA3 is considered the claimed buffer differential amplifier with the outputs connected in common then its inputs are not coupled to the pair of bit lines and if SA2 is considered the claimed buffer differential amplifier with its inputs coupled to the pair of bit lines then its outputs are not connected in common. Here, we agree with appellants that Watanabe does not anticipate

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the invention as recited in claim 37 based upon the examiner's statement of the basis of the rejection as recited in the supplemental answer. Therefore, we cannot sustain the examiner's rejection of claim 37 based upon 35 U.S.C. § 102.

CONCLUSION

To summarize, the decision of the examiner to reject claim 1 under 35 U.S.C. § 103 is reversed, and the decision of the examiner to reject claim 37 under 35 U.S.C. § 102 is reversed.

REVERSED

JERRY SMITH)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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JOSEPH L. DIXON)	
Administrative Patent Judge)	

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JLD:pgg
FOLEY & LARDNER
3000 K STREET, N.W., SUITE 500
P.O. BOX 25696
WASHINGTON , DC 20007-8696

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APPLICATION NO. 08/251,649

APJ DIXON

APJ JERRY SMITH

APJ BARRETT

DECISION: **REVERSED**

Prepared By: ????

DRAFT TYPED: 17 Oct 01

FINAL TYPED: