

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 34

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte RICHARD L. SITES  
and RICHARD T. WITEK

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Appeal No. 96-4033  
Application No. 08/086,354<sup>1</sup>

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ON BRIEF

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Before URYNOWICZ, THOMAS, and TORCZON, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 11 and 13-21. Claims 1 and 3-10 are allowed by the examiner in view of

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<sup>1</sup> Application for patent filed July 1, 1993. According to appellants, this application is a continuation of Application 07/547,589 filed June 29, 1990, now abandoned.

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arguments presented in the appeal brief. Claims 2 and 12 have been canceled.

The invention pertains to a data processor. Claim 11, the only independent claim before us on appeal, is illustrative and reads as follows:

11. A processor comprising:

means for executing a sequence of instructions of fixed length having sequential addresses, and detecting a conditional branch instruction in said sequence, said branch instruction having an opcode and a signed displacement;

means for detecting the sign of said displacement in said branch instruction;

means for (a) fetching a next instruction of said sequence, said next instruction having an address in sequence with said branch instruction, if said detected sign of said displacement is positive, or (b), in the alternative, fetching a branch target instruction not in said sequence, said target instruction having an address determined by said displacement, if said detected sign of said displacement is negative;

and means for testing a register defined in said branch instruction to determine a condition specified by said opcode, after said means for fetching has started fetching said next instruction or said branch target instruction.

The reference relied upon by the examiner as evidence of obviousness is:

Lee et al. (Lee)

4,755,966

July 5, 1988

The appealed claims stand rejected as under 35 U.S.C. § 103 as being unpatentable over Lee.

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The respective positions of the examiner and the appellant with regard to the propriety of these rejections are set forth in the final rejection (Paper No. 22) and the examiner's answer (Paper No. 29) and the appellants' brief (Paper No. 28) and reply brief (Paper No. 30).

#### Appellants' Invention

The invention relates to apparatus for efficient branching in a central processing unit. The apparatus makes use of unused bits in the opcode<sup>2</sup> of a computer instruction to provide a hint of an expected target address for branch and jump instructions. Because target address bits are stored in the computer instruction, the target can be prefetched before the actual address has been calculated and placed in a register. If the target address of the hint matches the calculated address when the instruction is actually executed, then the access of the data

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<sup>2</sup> "Opcode" is short for "operation code" and relates to the execution of an instruction. An "operation code" is a recognized term of art setting forth the list of operation parts in an instruction, together with the names of the corresponding operations.

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of the prefetched address has already been initiated and access time is reduced.

#### The Prior Art

Lee also relates to apparatus for conditional branching in a central processing unit (CPU). In discussing the background of the invention at column 1, lines 39-46, Lee discloses that "When a conditional branch instruction is executed with the condition true, it causes the CPU to continue execution at a new address referred to as a target address. Since instruction fetching is going on simultaneously with instruction decoding and execution in a pipelined computer, the computer has already fetched the instruction following the branch instruction in the program." The CPU must hold up the instruction pipeline following the branch instruction until the outcome of the branch instruction is known and the proper instruction is fetched (column 1, lines 48-51).

#### The Rejection under 35 U.S.C. §103

We note that, except for claim 21, appellants have not specifically argued the patentability of any dependent claim, indicating how it defines appellants' invention over the prior art. Accordingly, appellants' dependent claims 13-20 stand or

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fall with independent claim 11. In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987).

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that the rejection of claims 11 and 13-20 should be sustained but that the rejection of claim 21 should not be sustained. With respect to claim 11, we agree in general with the comments made by the examiner; we add the following discussion for emphasis.

At pages 12 and 13 of their brief, appellants contend that,

Appellants' claim 11 is likewise patentably distinct over Lee, which neither describes nor suggests "...means for fetching a next instruction of said sequence...having an address in sequence with said branch instruction if said detected sign of said displacement is positive or...fetching a branch target instruction...if said detected sign of said displacement is negative...and means for testing a register defined in said branch instruction to determine a condition specified by said opcode..."

The examiner contends at page 3, item (11), of the answer to the effect that the first element of claim 11 is met by Lee's disclosure at col. 2, lines 62-68, col. 3, lines 5-22 and 39-61, and col. 4, lines 26-41. The examiner further contends to the effect that the second and third elements of claim 11 are

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disclosed in Lee at col. 1, lines 8-11, col. 3, lines 5-11, col. 4, lines 64-68, col. 5, lines 1-20 and the claims. In item (12), the examiner asserts that Lee does not specifically detail the fourth and last element of claim 11 recited as means for testing a register defined in a branch instruction after fetching for the next instruction has started. In connection therewith, it is asserted to the effect that it was well-known in the art that in a pipeline system, while one instruction is being fetched, the instruction just prior to said one instruction is being executed, and the result of the execution of a third instruction in the pipeline just prior to the second instruction is being saved. At the top of page 4 of the answer, the contention is made that it was known to test a register defined for storing executed instruction results in instruction processing systems, and at page 5, the examiner takes the position that testing a register defined by the branch is nothing more than comparing the contents of the registers defined by the opcode field, which is taught by Lee at col. 1, lines 46-55. Lastly, the examiner contends the background art discussed by Lee discloses testing a register defined by the branch instruction to determine a condition defined by the opcode.

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In their reply brief, appellants argue that at col. 1, lines 46-55, Lee neither describes nor suggests "means for testing a register defined in said branch instruction to determine a condition specified in said opcode, after said means for fetching has started fetching said next instruction..." as recited in claim 11.

Appellants do not contend that Lee does not teach the first and second elements of claim 11, and we are convinced that these elements are in fact disclosed by the reference.

With respect to the third element of claim 11 defining means for fetching a next instruction or, in the alternative, a branch target instruction, this subject matter is taught by Lee at column 1, lines 6-15, wherein it is disclosed that the decision to branch or not to branch may be based on one or more events which include positive and negative numbers. In their reply brief, appellants have not challenged the examiner's position at page 3 of the answer to the effect that this disclosure satisfies the third element of the claim.

Regarding the fourth element of claim 11, at page 4, lines 11-21, appellants do not contend that Lee does not teach means for testing a register identified in a branch instruction to

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determine a condition specified by the opcode, but argue that the disclosure in Lee at column 1, lines 39-55, relied on by the examiner, does not teach means for testing the register after the means for fetching has started fetching the next instruction or the branch target instruction.

We do not find a clear teaching of comparing the contents of registers defined by the opcode field in col. 1, lines 39-55, of Lee, and the examiner has not explained how one would extrapolate such a teaching from this specific disclosure. Nevertheless, at column 1, lines 63 to column 2, line 9, Lee discloses that some prior art architectures have fetched both the instruction in the program following the branch instruction and the instruction at the branch target address together. In such a system, when a register identified in the branch instruction is tested or sampled to determine the condition specified by the operations code for execution of the branch instruction, that step can only be performed at the same time or after fetching of the instruction after the branch instruction has started or the fetching of the branch target instruction has started. Because 35 U.S.C.

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§ 103 requires us to presume that the artisan has full knowledge of the prior art in his field of endeavor, In re Deminski, 796 F.2d 436, 442, 230 USPQ 313, 315 (Fed. Cir. 1986), it would have been obvious to one of ordinary skill in the art to which the invention pertains to perform the above step after fetching the next instruction or the branch target instruction.

Whereas we will sustain the rejection of claim 11 over Lee and dependent claims 13-20 are not separately argued, we will sustain the rejection of claims 13-20 over Lee.

Because the examiner has made no specific showing of unpatentability of dependent claim 21, and appellants have shown that Lee does not teach or suggest either of the two elements added by the claim to the subject matter of claim 11 from which it depends, we will not sustain the rejection of claim 21.

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No period for taking any subsequent action in connection  
with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

STANLEY M. URYNOWICZ, JR.	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
JAMES D. THOMAS	)	APPEALS
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	)	INTERFERENCES
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AFFIRMED-IN-PART

Prepared: July 18, 2000