

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte HOLGER HEIL, JOSEF-MATTHIAS GANTIOLER  
and RAINALD SANDER

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Appeal No. 1996-4200  
Application No. 08/330,341<sup>1</sup>

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HEARD: October 20, 1999

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Before HAIRSTON, LALL, and GROSS, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 4. Appellants' Amendment After Final (paper number 13) amending claims 1 and 4, and canceling claims 2 and 3 was

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<sup>1</sup> Application for patent filed October 27, 1994.

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entered by the examiner (paper number 16). Accordingly,  
claims 1 and 4 remain before us on appeal.

The disclosed invention relates to an integrated  
comparator circuit.

Claim 1 is illustrative of the claimed invention, and it  
reads as follows:

1. An integrated comparator circuit, comprising:  
first and second terminals for a supply voltage;  
first and second input terminals;  
first, second, third and fourth MOSFETs each having drain,  
source and gate terminals and a transfer characteristic curve;  
said first and second MOSFETs being connected in a series  
circuit between said first terminal for the supply voltage and  
said first input terminal, defining a node between said first  
and second MOSFETs being connected to the gate terminal of  
said fourth MOSFET;  
said second input terminal being connected to said second  
terminal for the supply voltage;  
said third and fourth MOSFETs being connected to form and  
[sic] inverter stage between said first and second terminals  
for the supply voltage;  
the transfer characteristic curve of said second MOSFET being  
steeper than the transfer characteristic curve of said fourth  
MOSFET;  
said second and fourth MOSFETs each being an enhancement  
MOSFET;

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said first and third MOSFETs each being a depletion MOSFET;  
and

all of said MOSFETs being of the same channel type and all of  
said MOSFETs having a bulk terminal connected to said second  
terminal for the supply voltage.

The references relied on by the examiner are:

Van Zeghbroeck	4,771,194	
Sept. 13, 1988		
Leipold et al. (Leipold)	5,434,521	July
18, 1995		
	(filed Nov. 19,	
1992)		

Claims 1 and 4 stand rejected under 35 U.S.C. § 103 as  
being unpatentable over Leipold in view of Van Zeghbroeck.

Reference is made to the brief and the answer for the  
respective positions of the appellants and the examiner.

#### OPINION

The obviousness rejection of claims 1 and 4 is reversed.

The examiner acknowledges (Answer, page 3) that Leipold  
differs from the claimed invention in that Leipold uses "CMOS  
field effect transistors, while the appellants' invention uses  
four MOSFETS of the same channel type, i.e., n-type FETs."  
Leipold does not disclose the type of transistors used in his  
circuit [but we presume that they are all of the enhancement

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type], and only transistor 4 disclosed by Liepold has a bulk terminal connected to the second terminal for the supply voltage. Although the gate and drain terminals of transistor 1 in Liepold are interconnected, the gate terminal of transistor 3 is not interconnected to either the source terminal or the drain terminal.

The examiner is of the opinion (Answer, page 3) that it would have been obvious to one of ordinary skill in the art to substitute the four n-type FETs of Van Zeghbroeck in the Liepold comparator "since to switch the CMOS inverter of Liepold et al with inverter 26 of Van Zeghbroeck, and also to switch the diode-connected CMOS transistors 1, 2 of Liepold with the two n-type FETs 30, 31 of Van Zeghbroeck would enable a less complex manufacturing process for the Liepold et al comparator circuit." For additional justification for the modification, the examiner notes (Answer, page 4) that "the references have corresponding structures," that "the two references are directed to a similar technological field," and that "the FETs 30 and 36' in Van Zeghbroeck are depletion type FETs, whereas the FETs 31 and 37 are enhancement type FETs (similar to appellants' FETs 1, 3 and 2, 4)." With respect to

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the claimed bulk terminals all connected to the second terminal, the examiner is of the opinion (Answer, page 4) that it is well known in the art to do this "for purposes of convenience." The examiner does not offer any comments concerning the obviousness of interconnecting the gate and source terminals of transistors 1 and 3.

Appellants argue (Brief, pages 11, 14 and 15) that it would not have been obvious to the skilled artisan to apply the digital sense amplifier teachings of Van Zeghbroeck to the analog comparator teachings of Leipold. Even if they are combined, "Van Zeghbroeck does not teach all of the MOSFETs having a bulk terminal connected to said second terminal for the supply voltage as claimed in claim 1" (Brief, page 11), and "[t]he changes to the circuit of Leipold et al. necessary to create an operative circuit with MOSFETs of the same channel type [claims 1 and 4] from Van Zeghbroeck would not have been obvious from the cited Leipold et al. and Van Zeghbroeck references because neither reference shows or suggests the necessary changes to the circuit" (Brief, pages 12, 13 and 15). Although the examiner never addressed the gate and source terminal connections of the first and third

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transistors, the appellants argue (Brief, page 14) that Leipold "does not show either depletion MOSFETs [claims 1 and 4] or the gate and source terminals of the first and third MOSFETs being interconnected [claim 4]." In summary, appellants argue (Brief, page 17) that the teachings and suggestions of Van Zeghbroeck may not be combined with those of Leipold because there is no "teaching or suggestion to do so."

We agree with appellants that the examiner has not pointed to anything in the record or presented a convincing line of reasoning that would buttress his conclusions concerning the combinability of the disparate teachings in the applied references. Although Van Zeghbroeck discloses depletion-type FETs 30 and 36' (Figure 3) with gate terminals connected to drain/source terminals, the examiner has not provided any explanation as to how such circuit structure would be implemented in Leipold without adverse changes to the operation of the Leipold comparator. Even if we assume for the sake of argument that it would have been obvious to the skilled artisan to combine the teachings of the applied references, the combined teachings would still lack "all of

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said MOSFETs being of the same channel type" (claims 1 and 4), and "all of said MOSFETs having a bulk terminal connected to said second terminal for the supply voltage (claim 1).

In summary, we are of the opinion that the examiner has fallen victim to the use of impermissible hindsight in demonstrating the obviousness of the claimed invention. The obviousness rejection of claims 1 and 4 is, therefore, reversed.

#### DECISION

The decision of the examiner rejecting claims 1 and 4 under 35 U.S.C. § 103 is reversed.

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No period for taking any subsequent action in connection  
with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
PARSHOTAM S. LALL	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
	)	
ANITA PELLMAN GROSS	)	
Administrative Patent Judge	)	

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APJ HAIRSTON

APJ GROSS

APJ LALL

DECISION: REVERSED  
Send Reference(s): Yes No  
or Translation (s)  
Panel Change: Yes No  
Index Sheet-2901 Rejection(s): \_\_\_\_\_

Prepared: June 14, 2000

Draft    Final

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PALM / ACTS 2 / BOOK  
DISK (FOIA) / REPORT