

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ATSUSHI TAKASUGI

Appeal No. 1997-0013
Application No. 08/141,664

ON BRIEF

Before HAIRSTON, FLEMING, and HECKER, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 19. In an Amendment After Final (paper number 13), claims 1, 3, 4, 6, 9, 15 and 17 were amended.

The disclosed invention relates to a serial access memory that operates to convert the most significant bit of an

address data signal.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A serial access memory, comprising:
 - a first memory cell array including a plurality of memory cells each storing data therein, and a plurality of first word lines for applying respective first selection signals to the respective memory cells;
 - a second memory cell array including a plurality of memory cells each storing data therein, and a plurality of second word lines for applying respective second selection signals to the respective memory cells;
 - a first data register, coupled to the first memory cell array, for latching the data transferred from the first memory cell array;
 - a second data register, coupled to the second memory cell array, for latching the data transferred from the second memory cell array;
 - a first address decoder, connected to the first memory cell array, for outputting the first selection signals selectively to the first word lines, so as to select any of the first word lines in response to first address data applied to said first address decoder;
 - a second address decoder, connected to the second memory cell array, for outputting the selection signals selectively to the second word lines,

so as to select any of the second word lines in
response to second address data applied to said
second address decoder; and

less than the predetermined
portion which specifies addresses equal to or greater
than the predetermined address value, for converting
the most significant bit of the address data to a
predetermined
bit value, applying the first portion of the address
data, including the predetermined bit value, to the
first address decoder as the first address data at a
time that the data is transferred from the first and
second memory cell arrays respectively to the first
and second registers, and simultaneously applying
the second portion of the address data, including
the predetermined bit value, to the second address
decoder as the second address data.

The references relied on by the examiner are:

Shimizu	5,301,162	Apr. 5, 1994 (filed Mar. 23, 1993)
Watanabe et al. (Watanabe) 1994	5,319,603	Jun. 7, (filed Dec. 24, 1991)
Kaneko et al. (Kaneko) 1992 (published Japanese Kokai Patent Application)	4-275592 ¹	Oct. 1,

Claims 1, 3, 4, 6, 8, 9, 11 through 13 and 19 stand
rejected under 35 U.S.C. § 103 as being unpatentable over
Shimizu in view of Watanabe.

¹ A copy of the translation of this reference is attached.

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Claims 2, 5, 7, 10 and 14 through 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kaneko in view of Shimizu and Watanabe.

Reference is made to the briefs and the answer for the respective positions of the appellant and the examiner.

OPINION

The obviousness rejection of claims 1 through 19 is reversed.

The examiner is of the opinion that Shimizu discloses all of the claimed structure except for the conversion of the most significant bit (Answer, pages 3, 4 and 8). The examiner states (Answer, page 8) that "although Shimizu does not teach the conversion of the most significant bit, . . . Watanabe clearly teaches the conversion of the most significant bit as previously analyzed in the rejection." The examiner's previous analysis of the teachings of Watanabe was that "Watanabe teaches means for controlling the most significant bit to convert the input address data to first address data (0-127) and second address data (128-255); see column 10, lines 55-58" (Answer, page 4). The examiner concludes (Answer, pages 4 and 5) that "it would have been obvious to one of ordinary skill in the art to have used the most significant bit for transferring the input address data as taught by Watanabe to the memory device of Shimizu because the transferring operation with the most significant bit set would provide high speed processing."

The referenced portion of Watanabe (column 10, lines 55 through 58) states that "[t]he divided SAM(U) and SAM(L) correspond to '1' and '0' of the most significant bit (MSB) of a TAP address,^[2] and can transfer data independently from each other."

Appellant argues (Reply Brief, page 2) that:

Watanabe does disclose two RAM blocks transferring data to two SAM blocks according to the value of the most significant bit (MSB). However, the value of the MSB is simply observed and the SAM block designated for the transfer is chosen based on the value of the MSB as it was found . . . Therefore, the MSB of Watanabe is not converted to a predetermined bit value . . .

With respect to the referenced teachings of Watanabe, appellant argues (Reply Brief, page 3) that "Watanabe separates blocks of data based on the MSB, but does not 'use' the MSB for anything but block separation and identification."

We agree with appellant's arguments. Watanabe never converts the most significant bit of any type of address data. Thus, the obviousness rejection of claims 1, 3, 4, 6, 8, 9,

² Watanabe defines a tap address as "representative of the position of a new serial cycle after the data transfer" (column 1, lines 46 and 47).

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11 through 13 and 19 is reversed because Shimizu and Watanabe neither teach nor would they have suggested the conversion of a most significant bit of an address data signal (claims 1, 3, 4, 6, 8, 9 and 11) or the inverted and non-inverted most significant bit of the address signal (claims 12, 13 and 19).

The obviousness rejection of claims 2, 5, 7, 10 and 14 through 18 is reversed because the display teachings of Kaneko do not cure the noted shortcoming in the teachings of Shimizu and Watanabe.

DECISION

The decision of the examiner rejecting claims 1 through 19 under 35 U.S.C. § 103 is reversed.

REVERSED

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KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
MICHAEL R. FLEMING)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
)	
STUART N. HECKER)	

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Administrative Patent Judge)

KWH:hh

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Steven M. Rabin
1725 K. Street N.W., Suite 1111
Washington, D.C. 20006