

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EIJI IWATA

Appeal No. 1997-0201
Application No. 08/140,318

ON BRIEF

Before MARTIN, JERRY SMITH, and RUGGIERO, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 4-14, all of the claims pending in the present application. Claims 1-3 have been canceled. An amendment after final rejection was filed February 27, 1996 and was entered by the Examiner.

The disclosed invention relates to a processing circuit for detecting and processing a motion vector used for picture

compression and encoding. More particularly, Appellant indicates at pages 14 through 16 of the specification that a block-matching procedure is utilized for finding a candidate block within a search range of a previous frame which bears the strongest resemblance to a reference block in a current frame. The motion vector is determined by calculating a positional shift between the blocks in the current and previous frames.

Claims 4 and 7 are illustrative of the invention and read as follows:

4. A processing circuit for performing motion detection by dividing picture-based image signals into blocks, each block comprising a pre-set number of pixels and for searching for an entire picture utilizing a block-matching method, with the block size of a reference block of the current picture comprising $M \times N$ pixels and with the number of candidate blocks of a previous picture being $M \times N$, said circuit comprising

a plurality of processing units equal in number to the product $M \times N$, each of said processing units being adapted for calculating an evaluation value based on a difference between a pixel value of said reference block and a pixel value of a one of said candidate blocks under consideration, said processing units being arrayed in a $M \times N$ matrix configuration, outputs of said processing units being connected in a pipeline configuration via a plurality of additive nodes, the pixel values of said reference block and the pixel values of said one candidate block under consideration being processed in a pre-set sequence to thereby

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detect a motion vector based on the evaluation value of said difference.

7. A processing circuit for performing motion detection by dividing picture-based image signals into blocks, each block comprising a pre-set number of pixels and for searching an entire picture utilizing a block-matching method, wherein the block size of a reference block of the current picture comprises $M \times N$ pixels and the number of candidate blocks of a previous picture being $M \times N$, said circuit comprising:

a plurality of processing units equal to the product of $M \times N$, each of said processing units being adapted for calculating an evaluation value based on a difference between a pixel value of said reference block and a pixel value of a one of said candidate blocks under consideration, and for summing said evaluation values, said processing units being arrayed and interconnected in an $M \times N$ matrix configuration, the pixel values of said reference block and the pixel values of the candidate block under consideration being input to said processing units in a pre-set sequence to thereby detect a motion vector;

wherein each picture is a frame and wherein each processing unit comprises:

a register for sequentially storing the pixel values of a current frame,

a multiplexer for multiplexing pixel values of an odd column of a previous frame which is under consideration with the pixel values of an even column of the previous frame which is under consideration,

a processor for calculating an absolute value of the difference between an output of said register and an output of said multiplexer, and

an accumulator for accumulating outputs of said processor for summing the absolute values of the differences.

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The Examiner relies on the following prior art:

Komarek et al. (Komarek), "Array Architectures for Block Matching Algorithms," IEEE Transactions on Circuits and Systems, vol. 36, no. 10 (October 1989).

De Vos et al. (De Vos), "Parameterizable VLSI Architectures for the Full-Search Block-Matching Algorithm," IEEE Transactions on Circuits and Systems, vol. 36, no. 10 (October 1989).

Claims 4-14 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Komarek in view of De Vos.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Brief and Answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellant's arguments set forth in the Brief along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

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It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 4-6, 12, and 14. We reach the opposite conclusion with respect to claims 7-10, 11, and 13. Accordingly, we affirm-in-part.

Appellant has indicated (Brief, pages 9 and 10) that, for the purposes of this appeal, claims 4 and 7 through 10 stand or fall separately. We will consider the claims separately only to the extent that separate arguments are of record in this appeal. Dependent claims 5, 6, and 11-14 have not been argued separately and, accordingly, will stand or fall together with their base claim.

As a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to Appellant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the

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arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Arguments which Appellant could have made but elected not to make in the Brief have not been considered in this decision (note 37 CFR § 1.192).

In making the obviousness rejection, the Examiner has grouped all of the appealed claims together and asserts that the combination of Komarek and De Vos would suggest to the skilled artisan the obviousness of the claimed invention. Although the Examiner included independent claim 4 in the obviousness rejection based on the combination of Komarek and De Vos, it is apparent from the statement of the grounds of rejection (Answer, page 3 which references a previous Office action, paper no. 7 mailed July 3, 1995) that the Examiner considers Komarek alone to teach all of the claim 4 limitations.

In response, Appellant attacks the Examiner's characterization of the processing element array in Komarek as

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being connected in a pipeline configuration. We note that the relevant portion of claim 4 recites:

outputs of said processing units being
connected in a pipeline configuration
via a plurality of additive nodes,...

Upon careful review of the Komarek reference, we are in agreement with the Examiner that the processing units in Figure 1 of Komarek are "pipelined" through additive nodes at least in the manner broadly recited in the claims. While Appellant has focused his arguments on the alleged deficiencies of the fan-out configuration of Komarek's Figure 4, it is apparent to us that the Figure 1 illustration of Komarek, also relied on by the Examiner, clearly describes the outputs of processing elements being "pipelined" down to additive nodes, the outputs of which are added to the outputs of other processing elements. We are further persuaded by the Examiner's citation of various portions of Komarek which suggest the apparent practical necessity of utilizing pipeline processing for implementing block-matching algorithms (Komarek, p. 1302, left and right hand columns, last paragraph). In our view, the Examiner's analysis and line of reasoning establishes a prima facie case of anticipation which

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remains un rebutted by any convincing arguments of Appellant. A disclosure that anticipates under 35 U.S.C. § 102 also renders the claim unpatentable under 35 U.S.C. § 103, for "anticipation is the epitome of obviousness." Jones v. Hardy, 727 F.2d 1524, 1529, 220 USPQ 1021, 1025 (Fed. Cir. 1984). See also In re Fracalossi, 681 F.2d 792, 794, 215 USPQ 569, 571 (CCPA 1982); In re Pearson, 494 F.2d 1399, 1402, 181 USPQ 641, 644 (CCPA 1974). Thus, we sustain the Examiner's 35 U.S.C. § 103 rejection of independent claim 4 as well as claims 5, 6, 12, and 14 dependent thereon and not separately argued by Appellant.

Turning now to a consideration of independent claims 7 and 8, grouped and argued separately by Appellant, we note that, while we found Appellant's arguments to be unpersuasive with respect to the obviousness rejection of independent claim 1, we reach the opposite conclusion with respect to independent claims 7 and 8. In addition to claiming various hardware elements (i.e. register, multiplexer, and accumulator) which constitute the claimed processing units, these claims also specifically recite the operation of multiplexing pixel values of odd and even columns of a

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previous frame under consideration. The Examiner (Answer, page 4) has attempted to address this claim language by, initially, suggesting the inherency and conventionality of the recited hardware components in the processing elements of Komarek, further relying on Figures 4 and 5 of De Vos as evidence of such assertion. Further, the Examiner suggests that the MUX operation illustrated in Figure 4 of De Vos which is described as selecting previous frame line data in increments of 1, m times would necessarily multiplex odd and even columns of pixels. Notwithstanding the merits of the Examiner's general contention as to the inherency of the inclusion of registers, multiplexers, and accumulators in processing elements, we find Appellant's arguments to be persuasive with respect to the claimed multiplexing of odd and even columns of pixels. Aside from the bare, general description of incrementing previous frame line data in De Vos, the Examiner has pointed to no disclosure which would lend support to the conclusion that odd and even pixel column multiplexing is necessarily performed in De Vos. To the contrary, as pointed out by Appellant (Brief, page 17), the "meander" scheme described at page 1312 of De Vos can only

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reasonably lead to the conclusion that, in a given cycle, data from only even or odd columns are processed, rather than being multiplexed as claimed. We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a prima facie case. In re Knapp-Monarch Co., 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); In re Cofer, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966).

Accordingly, since all of the limitations are not taught or suggested by the prior art, we do not sustain the obviousness rejection of independent claims 7 and 8, nor of claims 11 and 13 dependent thereon. Dependent claims 9 and 10 also contain the limitations regarding the multiplexing of odd and even pixel columns and we do not sustain the obviousness rejection of these claims as well.

In summary, we have sustained the 35 U.S.C. § 103 rejection of claims 4-6, 12, and 14, but have not sustained the 35 U.S.C. § 103 rejection of claims 7-11, and 13

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Therefore, the Examiner's decision rejecting claims 4-14 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JOHN C. MARTIN)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JERRY SMITH)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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APJ MARTIN

DECISION: AFFIRMED-IN-PART
Send Reference(s): Yes No
or Translation (s)
Panel Change: Yes No
Index Sheet-2901 Rejection(s):

Prepared: April 20, 2001

Draft Final

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OB/HD GAU

PALM / ACTS 2 / BOOK
DISK (FOIA) / REPORT