The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD BOWERS

Appeal No. 1997-0706
Application No. 08/040,528

ON BRIEF

Before RUGGIERO, DIXON, and BARRY, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1-21. An amendment after final rejection filed February 16, 1996 which canceled claims 5, 11, and 17 was entered by the Examiner. A further amendment after final rejection dated November 6, 1996, which accompanied

Appellant's filing of the Reply Brief, was also entered by the Examiner. At page 2 of the Answer, the Examiner indicted the withdrawal of the rejection of claims 2-4, 8-10, 14-16, 20, and 21. Accordingly, only the rejection of claims 1, 6, 7, 12, 13, 18, and 19 is before us on appeal.

The claimed invention relates to a multiple use chip socket in which first and second types of chips can be supported in a single chip socket. The particular type of chip installed in the socket is determined by control logic that reads a predetermined memory location of the chip. Addressing signals are selectively applied to the chip socket by the control logic depending on the type of chip determined to be installed in the socket.

Claim 1 is illustrative of the invention and reads as follows:

1. A multiple use chip socket comprising:

a chip socket for receiving either a first chip type or a second chip type, said first chip type having a first set of signals, said second chip type having a second set of signals different from said first set of signals; and

control logic coupled to said chip socket for determining whether a chip of said first chip type or said second chip type is installed in said chip socket by reading a predetermined memory location of a chip installed in said chip socket and for providing signals to said chip socket

compatible with either said first set of signals or said second set of signals to configure said chip socket to support operation of either said first chip type or said second chip type installed in said chip socket.

The Examiner's Answer cites the following prior art references:

Powell	4,319,343	Mar. 09, 1982
Chuang	5,546,563 (effectively filed Apr. 22, 1991)	Aug. 13, 1996

As a result of a new ground of rejection in the Answer, claims 1, 6, 7, 12, 13, 18, and 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Chuang.[1]

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Briefs[2] and Answer, as well as to the Examiner's comments in the attachment to the

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[1] Although the Examiner, in the final Office action, had made a prior art rejection based on Powell, no mention of this rejection is made in the Examiner's Answer or in the attachment to the Advisory action (Paper No. 28, mailed October 14, 1999), which responds to Appellant's Reply Brief. We conclude, therefore, that the rejection based on Powell has been withdrawn. See Ex parte Emm, 118 USPQ 180, 181 (Bd. App. 1957).

[2] The Appeal Brief (revised) was filed July 25, 1996. In response to the Examiner's Answer dated October 17, 1996, a Reply Brief was filed November 6, 1996 which was entered and discussed by the Examiner in the Advisory action mailed October 14, 1999.

Advisory action mailed October 14, 1999 (Paper No. 28) for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner and the evidence of anticipation relied upon by the Examiner as support for the rejection. We have likewise reviewed and taken into consideration, in reaching our decision, Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer and in the attachment to the Advisory action of October 14, 1999.

It is our view, after consideration of the record before us, that the disclosure of Chuang does not fully meet the invention as set forth in claims 1, 6, 7, 12, 13, 18, and 19. Accordingly, we reverse.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied

Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

With respect to independent claims 1 and 7, the Examiner, at pages 3 and 4 of the Answer, attempts to read the various claim limitations on the Chuang reference. In particular, the Examiner points to the chip socket 10 and control logic circuitry 14 illustrated in Chuang's Figure 2.

In response, Appellant's primary argument (Reply Brief, page 2) centers on the contention that Chuang fails to disclose the determination of a particular chip type installed in the chip socket "by reading a predetermined memory location of a chip installed in said chip socket" as claimed. After careful review of the Chuang reference in light of the arguments of record, we are in agreement with Appellant's position as stated in the Reply Brief.

We agree with Appellant that, while Chuang utilizes a signal (MP#) emanating from a particular socket pin, i.e., pin 31, for chip type identification, there is no indication from the disclosure of Chuang that this signal is associated

with the reading of a predetermined memory location of an installed chip. Although the Examiner, in the attachment to the Advisory action of October 14, 1999, suggests the inherency of the assignment of particular socket pin numbers to predetermined locations of the installed chip memory, the record is totally devoid of any support for such an assertion. To establish inherency, evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference and would be recognized as such by persons of ordinary skill. In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) citing Continental Can Co. v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Id. citing Continental, 948 F.2d at 1269, 20 USPQ2d at 1749.

In view of the above discussion, since all of the claimed limitations are not disclosed by Chuang or inherent therein, the Examiner's 35 U.S.C. § 102(e) rejection of independent

claims 1 and 7, as well as claims 6, 12, 18, and 19 dependent thereon, cannot be sustained.

Turning to a consideration of independent claim 13, we do not sustain the Examiner's 35 U.S.C. § 102(e) rejection of this claim as well. While claim 13 does not include a recitation of determining chip type by reading a predetermined memory location of an installed chip, there is a clear, specific recitation of a step of determining whether an installed chip "is required to be accessed as a boot device." We find no disclosure of any such feature in Chuang, nor do we find any indication from the Examiner's line of reasoning as to how the disclosure of Chuang could be interpreted as meeting such claim limitation.

In conclusion, we have not sustained the Examiner's 35 U.S.C. § 102(e) rejection of any of the claims on appeal. Accordingly, the Examiner's decision rejecting claims 1, 6, 7, 12, 13, 18, and 19 is reversed.

REVERSED

Joseph F. Ruggiero)
Administrative Patent Judge)
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Joseph L. Dixon Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
Lance Leonard Barry Administrative Patent Judge	)

JFR:tdl

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