

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte DAVID C. McCLURE

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Appeal No. 1997-1060  
Application No. 08/172,848<sup>1</sup>

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ON BRIEF

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Before HAIRSTON, FLEMING and LALL, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-37, which represents all of the claims remaining in the application.

The invention pertains to a method and system for testing a packaged semiconductor memory device to determine whether

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<sup>1</sup> Application for patent filed December 22, 1993.

redundant rows and columns have been implemented on the semiconductor memory device. More specifically, through external pins on the packaged semiconductor memory device, three redundancy rollcall tests are performed on the device to determine whether redundancy has been implemented, and to identify the row addresses and the column addresses at which redundancy has been implemented.

Claims 1, 11 and 37<sup>2</sup> are illustrative of the claimed invention, and read as follows:

1. A method of testing a packaged semiconductor memory device to acquire information on redundant elements, said method comprising the steps of:

configuring the device in a test mode; and  
in response to configuring the device into a first test mode, sensing a first programmed signal indicating that redundancy has been implemented on the device, and changing the state of at least one output pin when the first signal has a preselected value.

11. A method of testing a semiconductor device to acquire information on redundant elements, said method comprising the steps of:

configuring the device for at least one test mode;

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<sup>2</sup> In claim 37, line 7, it appears that the phrase "first signal" should read -programmed signal--. This informality should be corrected in any further prosecution that may occur.

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sequentially addressing selected cells of the device;  
changing the state of at least one device output if a  
redundant line has been addressed.

37. A method of testing a semiconductor device to  
determine whether redundancy implementation has occurred on  
redundant elements within the semiconductor device, the method  
comprising the steps of:

configuring the device in at least one test a [sic] mode;

sensing a programmed signal indicating whether redundancy  
has been implemented on the device; and

changing the state of at least one device output when the  
first signal has a predetermined value, wherein whether  
redundancy implementation of redundant elements in the  
semiconductor memory device is indicated by the changed state  
of the at least one device output.

The prior art relied upon by the examiner is:

Saito et al. (Saito)	4,860,260	Aug. 22, 1989
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The appealed claims stand rejected under 35 U.S.C. § 102  
or § 103 as follows:

a) claims 1-6, 11-15, 28-33 and 37-40 under 35 U.S.C. §  
102 (b) as being anticipated by Saito; and

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b) claims 7<sup>3</sup>-10, 16-27<sup>4</sup>, and 34-36 under 35 U.S.C. § 103  
(a) as being unpatentable over Saito.

We make reference to the examiner's answer (Paper No. 14, mailed August 22, 1996) and the Office Action referred to therein for the examiner's reasoning in support of the rejections, and appellant's appeal brief and reply brief (Paper No. 13, filed May 20, 1996 and Paper No. 15, filed October 21, 1996, respectively) for appellant's arguments thereagainst.

#### OPINION

In reaching our decision in this appeal, we have given careful consideration to appellant's specification and claims, to the applied prior art references, and to the respective positions articulated by appellant and the examiner. As a

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<sup>3</sup> In claim 7, line 6, after "one" there appears to be a term missing from this line.

<sup>4</sup> In claim 27, line 4, "switching" should be changed to --changing--.

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consequence of our review, we have made the determinations which follow.

We will not sustain the examiner's rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by Saito.

Although we find that Saito teaches the steps of (1) "configuring the device in a test mode" (col. 5, lines 41-44) and (2) "sensing a first programmed signal indicating that redundancy has been implemented on the device" (col. 6, lines 16-38), we are in general agreement with the appellant (Brief, page 5) that Saito fails to teach the recited step of "changing the state of at least one output pin when the first signal has a preselected value." The examiner, on page 4 of the Answer, maintains that "substitution of a redundant element (blowing of a fuse)" is precisely on point with the Appellant's claimed "state change of the output of a pin." We do not agree. The appellant argues on page 6 of the brief that the output pin defined in claim 1 represents the output pin of the device. In contrast, a review of the teachings of Saito reveals that the step of blowing a fuse results in a

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change in state of an output of one of the elements within the semiconductor device rather than a change in state of an output pin of the semiconductor device. Therefore, the artisan would not have been placed in possession of the presently claimed invention defined by independent claim 1 as is required by 35 U.S.C. § 102. Accordingly, we will not sustain the examiner's rejection of claim 1 under 35 U.S.C. § 102(b). It follows that we also will not sustain the examiner's rejections of claims 2-6 and 8-10 based on Saito.

We now turn our attention to the rejection of claims 11 and 37 under 35 U.S.C. § 102(b) based on the disclosure of Saito.

Initially, we note that anticipation under 35 U.S.C. § 102 is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of the claimed invention. *See In re Schreiber*, 128 F.3d 1473, 1477, 44 USPQ 1429, 1431 (Fed. Cir. 1997); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990); *RCA Corp. v. Applied*

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*Digital Data Systems, Inc.*, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.), *cert. dismissed sub nom., Hazeltine Corp. v. RCA Corp.*, 468 U.S. 1228 (1984). However, the law of anticipation does not require that the reference teach specifically what an appellant has disclosed and is claiming. Anticipation merely requires that the claims on appeal "read on" something disclosed in the reference, *i.e.*, all limitations of the claim are found in the reference. See *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), *cert. denied*, 465 U.S. 1026 (1984).

With the above in mind, we note that both Saito and the appellant's claim 11 are directed toward a method of testing a semiconductor device that includes redundancy implementation. More specifically, after careful review of appellant's claim 11 and the teachings of Saito, we find that we are in general agreement with the examiner (Office Action mailed April 6, 1995) that appellant's limitation of "[a] method of testing a semiconductor device to acquire information on redundant elements" is taught in column 5, lines 55-68 and column 6,

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lines 39-65 of Saito. The appellant's claim 11 limitation of "configuring the device for at least one test mode" is met by applying the supply voltage ( $V_{cc}$ ) and supplying test signals **TEST 1** to **TEST M** to appropriate pads of the exchange controller. We also agree with the examiner that the appellant's claim 11 limitation of "sequentially addressing selected cells of the device" is met by the teachings in column 5, lines 41-43 and lines 55-67, and column 6, lines 65-67 of Saito. The appellant's claim 11 limitation of "changing the state of at least one device output if a redundant line has been addressed" is met by the change in state of the device output **RDE** from a high level signal to a low level signal when a redundant line has been addressed. (Column 5, lines 62-67 and column 6, lines 11-15). We are mindful of the fact that claims are to be given their broadest reasonable interpretation during prosecution. *In re Prater*, 415 F.2d 1393, 162 USPQ 541 (CCPA 1969). Consequently, unlike appellant's claim 1, claim 11 is not limited to changing the state of an external output pin on the semiconductor device. Quite the opposite, when we give claim 11 the broadest

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reasonable interpretation consistent with appellant's specification, we find that the limitation of ". . . changing the state of at least one device output if a redundant line has been addressed" covers any device output, even one located within the semiconductor device that changes state as a result of addressing a redundancy line. A close review of the disclosure of Saito reveals that prior to addressing a redundant line, **RDE** is held high for the purpose of enabling the row decoder (**32**). Saito specifically teaches in column 5, lines 49-67 and column 6, lines 11-15 that:

*Upon detection of the programmed row address signal AR, exchange controller **46** inhibits the selective operation of row decoder **32** and selects the row of redundancy memory cell array **30B** in accordance with the detected specified row address signal.*

The selecting operation of decoder **32** is enabled during the time period in which the control signal RDE is set at a high level and disabled during the time period in which the control signal RDE is set at a low level.

Accordingly, the change in state of output **RDE** on device (**54**) located within the semiconductor memory device meets the limitation of ". . . changing the state of at least one device output . . ." as required by claim 11.

Thus, we will sustain the examiner's rejection of claim 11 since all of the limitations required by claim 11 are found in Saito.

Turning now to claim 37, the limitation of "configuring the device in at least one test a [sic] mode" is again met by applying the supply voltage ( $V_{cc}$ ) and supplying test signals **TEST 1** to **TEST M** to appropriate pads on the exchange controller. The limitation of "sensing a programmed signal indicating whether redundancy has been implemented on the device" is met by any of address detectors **50-1** to **50-M**. The limitation of "changing the state of at least one device output when the first signal has a predetermined value, wherein whether redundancy implementation of redundant elements in the semiconductor memory device is indicated by the changed state of the at least one device output" is met by device (**54**) and the change in state of its output **RDE** when

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redundancy has been implemented on the semiconductor device.  
(column 5, lines 49-54, 62-67; column 6, lines 11-15; and  
column 7, lines 15-26).

Since the examiner's rejection of claims 11 and 37 has  
been affirmed, we likewise affirm the rejections of claims 7  
and 12-36 since these claims stand or fall (Brief, page 3)  
with representative claims 11 and 37, respectively, and the  
appellant has failed to provide any reasons why claims 7 and  
12-36 are believed to be separately patentable.

To summarize:

We have reversed the examiner's rejections of claims 1-6  
and 8-10.

We have affirmed the examiner's rejections of claims 7  
and 11-37.

#### DECISION

The decision of the examiner is affirmed-in-part.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136 (a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
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	)	BOARD OF
PATENT	)	
MICHAEL R. FLEMING	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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PARSHOTAM S. LALL	)	
Administrative Patent Judge	)	

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