

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAYAKAR C. REDDY,
MODUGU V. REDDY,
and KRISHNAN C. DHARMARAJAN

Appeal No. 1997-1197
Application 08/130,255¹

HEARD: December 6, 1999

Before HAIRSTON, BARRETT, and DIXON, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed October 1, 1993, entitled "Image Rotation For Video Displays."

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This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-4 and 7-19, and 22-26. Claims 5, 6, 27, and 28 stand objected to (Final Rejection, page 5). The amendment after final rejection (Paper No. 7) presumably overcomes the rejection of claims 20 and 21 under 35 U.S.C. § 112, second paragraph, so claims 20 and 21 presumably also stand objected to (Final Rejection, page 5).

We affirm-in-part.

BACKGROUND

The disclosed invention is directed to a method and apparatus for displaying and selectively rotating an image on an image display unit. An image is stored in memory in a certain sequence of bits, e.g., from a least significant bit (LSB) to a most significant bit (MSB) and from a low address to a high address as shown in figure 1. The image may be read out from memory in the same sequence to form a normal image on the display as shown in figure 1, or may be read out in an inverse sequence to form an inverted display as shown in figure 5.

Claim 1 is reproduced below.

1. Apparatus for displaying a video image on at least one video display, said video image stored as pixel

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data in a memory in a first sequence, said apparatus comprising:

scanning means, coupled to said memory and said at least one video display, for both reading image data from said memory in a prescribed sequence and scanning said image data to said video display in said prescribed sequence; and

selector means coupled to the scanning means for selecting a first sequence or a second sequence different from said first sequence as said prescribed sequence.

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The Examiner relies on the following prior art references:

Fujisawa et al. (Fujisawa)	4,926,166	May 15, 1990
Kajihara	4,929,085	May 29, 1990
Okazawa et al. (Okazawa)	5,034,733	July 23, 1991

Claims 1, 2, 9-12, and 15-17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kajihara.

Claims 7, 8, 13, 14, 18, and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kajihara and Okazawa.

Claims 3, 4, and 22-24 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kajihara and Fujisawa.

Claims 25 and 26 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kajihara, Fujisawa, and Okazawa.

We refer to the Final Rejection (Paper No. 6) (pages referred to as "FR__"), the Examiner's Answer (Paper No. 12) (pages referred to as "EA__"), and the communication² entered September 13, 1996 (Paper No. 15) for a statement of the Examiner's position and to the Appeal Brief (Paper No. 11) (pages referred to as "Br__") and the Reply Brief (Paper

² Which should be in the form of a "Supplemental Examiner's Answer."

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No. 13) (pages referred to as "RBr__") for a statement of
Appellants' arguments thereagainst.

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OPINION

Related case

We have considered our decision and decision on request for rehearing in Application 08/130,577, Appeal No. 96-1444, but do find them controlling on our decision in this case.

Anticipation

"Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention."

RCA Corp. v. Applied Digital Data Systems, Inc.,

730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

We confine our analysis to issues and differences argued in the brief. See 37 CFR § 1.192(c)(8)(iii) (1995) ("For each rejection under 35 U.S.C. 102, the argument shall specify the errors in the rejection and why the rejected claims are patentable under 35 U.S.C. 102, including any specific limitations in the rejected claims which are not described in the prior art relied upon in the rejection."). Cf. In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to

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examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art."); In re Wiechert, 370 F.2d 927, 936, 152 USPQ 247, 254 (CCPA 1967) ("This court has uniformly followed the sound rule that an issue raised below which is not argued in this court, even if it has been properly brought here by a reason of appeal, is regarded as abandoned and will not be considered. It is our function as a court to decide disputed issues, not to create them."); In re Wiseman, 596 F.2d 1019, 1022, 201 USPQ 658, 661 (CCPA 1979) (arguments must first be presented to the Board before they can be argued on appeal).

Claims 16 and 17

Appellants argue that Kajihara fails to show reading a frame of image pixel data from a memory in one of two sequences (Br12): "There is no indication that address generator 19 operates in other than a conventional manner (see col. 4, line 63, to col. 5, line 8). Thus, in Kajihara, the image data is read from buffer memory 15 in one sequence only."

The Examiner finds (EA7-8) that figures 2A-2D show that selector 54 of figure 1 can select one of four scan sequences

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and that figure 5 shows that selector 16 of figure 3 can select one of four scan sequences. In response to Appellants' argument that reliance on figure 1 is a new argument (RBr2-4), the Examiner states that he does not rely on figure 1 (Paper No. 15, page 2).

While the Examiner's rejection does little more than find that an image rotation generally takes place without addressing particularly how the claim limitations read on the complicated circuit of Kajihara, we nevertheless find that Kajihara anticipates claim 16. Specifically, we rely on the "output raster scan mode" wherein an image is read out from the page memory in accordance with a designated rotation angle as shown in figures 2A-2D and the rotated image data is subjected to rotation processing (col. 7, lines 16-25). The page memory is not shown in figure 3, but is described as the source of image data for the circuit. The page memory corresponds to the claimed "frame of pixel data" (as admitted by Appellants at Br16, lines 1-2; RBr8).

Consider the cases of 0-degree and 180-degree rotation. "When the 0-degree rotation command is input, words at addresses 0 [sic, 1] to 40 are read out from the page memory,

as shown in FIG. 2A, and are stored in buffer memory 15" (Col. 7, lines 35-38.) Because the bits of the words are output serially beginning with the LSB (e.g., col. 6, lines 25-26), the bits are output as, for example, word 1, bit 0 (LSB or rightmost bit), bit 1, . . . , bit 7 (MSB or leftmost bit), word 2, bit 0, bit 1, etc. This is a "sequence" of pixels (bits) as broadly claimed.

"When the 180-degree rotation command is input to controller 18, the words are read out from the page memory upon scanning as shown in FIG. 2C." (Col. 8, lines 15-17.) The words are read out in inverse order for the 180-degree rotation than from the 0-degree rotation. Because the bits of the words are output serially beginning with the LSB, the bits are output in sequence from the LSB of word 200 to the MSB of word 1. This is a "second sequence different from the first sequence."

Therefore, the page memory (storing a frame of pixel data) is selectively read in two different bit (pixel) sequences. Note that the rejection relies on the way the data is read out from the page memory before it goes to the circuit of figure 3. Because the output of Kajihara is word oriented,

the order of the bits of the words from the page memory must be reversed in the circuit of figure 3 so that when, say, word 200 is written to a display or memory in the position of word 1, during a 180-degree rotation, the bits are in the correct position. The fact that additional steps occur in the circuit of figure 3 is irrelevant to the anticipation rejection since claim 16 is open-ended and does not preclude other steps. Claim 16 does not recite that the image data is scanned to a display in the sequence it is read out; compare claim 1. The output of the figure 3 circuit goes to external apparatus (e.g., col. 8, lines 45-46) and Appellants do not contest that such apparatus includes a display. It is inherent that the pixels (bits) would be converted to unit drive signals in order to be displayed, but this is not argued.

Appellants also argue that buffer memory 15 in Kajihara does not store a frame of pixel data (Br12). The Examiner does not respond to this argument.

It is true that buffer memory 15 consists of RAM 1 and RAM 2, which each have a capacity of 40 words (where each word is eight bits). However, we rely on the page memory in

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figure 6, which holds 200 words, and is considered to correspond to memory storing a frame of pixel data. Claim 16 does not preclude the frame of pixel data from being read out a block at a time where the blocks correspond to the size of the RAMs.

For the reasons stated above, the rejection of claim 16 is sustained. Claim 17 is not separately argued and, therefore, falls with claim 16. The rejection of claim 17 is sustained.

Claims 1 and 2

Appellants argue that there is no reading out of image data from the memory in different sequences (Br14). We disagree for the reasons discussed in connection with claim 16, where the claimed memory corresponds to the page memory in Kajihara, not the buffer memory 15.

Appellants argue that "claim 1 requires that the image data be scanned on a video display in the same prescribed sequence that the image data is read out of memory" (Br13-14). The Examiner does not address this argument.

We find that Kajihara does not scan the image data in the same prescribed sequence that the image data is read out of

memory. As discussed in connection with claim 16, in the "output raster scan mode," for the 0-degree rotation, the words are read out from the page memory in sequential order (words 1, 2, ...) and since the words are output in a serial manner starting with the LSB, the bits of the word are output as, for example, word 1, bit 0 (the LSB), bit 1, ..., bit 7 (the MSB), word 2, bit 0, bit 1, etc. The bits are not subject to bit-order reversal or rotation (see figure 5 for 0E under output raster scan mode) and would be written to a display in the same order as read out from the page memory. For the 180-degree rotation, the words are read out in an inverse order (words 200, 199, ...). However, the bits are subject to bit-order reversal in the circuit of figure 3 (see figure 5 for 180E under output raster scan mode) and therefore would be written to a display in a different order than they were read out from the page memory. This is an artifact of the fact that Kajihara is a word-based system and not a bit-based system. Nevertheless, the rejection is based on anticipation and must be reversed because Kajihara does not meet the function of "scanning said image data to said video

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display in said prescribed sequence." The rejection of claims 1 and 2 is reversed.

Claims 9-12 and 15

Claim 9 is similar to claim 16 except that it is an apparatus claim expressed in means-plus-function language. Appellants argue that the means-plus-function terms must be interpreted in accordance with 35 U.S.C. § 112, sixth paragraph, in accordance with In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994) (in banc) and that the cited references do not disclose or suggest either the function or structural equivalents for the means described in the specification, such as in figures 10a and 10b (Br16-17). The Examiner responds that Donaldson is a newly-raised argument and that Appellants broadly disclose a black box structure in figures 8A and 8B which is equivalent to Kajihara (Paper No. 15, page 3). It was argued at oral hearing that the Examiner failed to properly interpret the claims under § 112, sixth paragraph. We have several answers to Appellants' arguments.

First, upon review of the prosecution history, we find that Donaldson was not raised until the remarks in the

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amendment after final rejection (Paper No. 7). Therefore, Appellants' raising the means-plus-function interpretation after the final rejection is untimely for purposes of this appeal. See In re Webb, 916 F.2d 1553, 1556, 16 USPQ2d 1433, 1435 (Fed. Cir. 1990) ("[A]n examiner's final rejection, which precipitates the statutory right to appeal to the Board, 35 U.S.C. § 134 (1988), constitutes the 'decision' of an examiner for purposes of § 1.196(a).").

Second, Appellants have failed to comply with the Office procedure for § 112, sixth paragraph, by showing that the prior art structure is not the same or an equivalent. See Examination Guidelines for Claims Reciting a Means or Step Plus Function Limitation In Accordance With 35 U.S.C. § 112, 6th Paragraph, 1162 Off. Gaz. Pat. & Trademark Office 59, 59-60 (May 17, 1994) (the examiner initially makes a prima facie case that a limitation is anticipated by showing that a prior art structure performs the function, then the burden of going forth with the evidence shifts to applicant to show that the prior art structure is not the same as or an equivalent of the structure, material, or acts described in the specification). Appellants merely assert that the Examiner has not shown that

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the structure in Kajihara is an equivalent, without particularly pointing out what structure in figures 10a and 10b is the structure required to perform the claimed functions or why the structure in Kajihara is not the same or an equivalent.

For these two reasons, the issue of structure and equivalents under § 112, sixth paragraph, should not be an issue in any judicial review. Without waiving this position, for Appellants' benefit we comment on why the means-plus-function language of claim 9 does not distinguish over Kajihara.

Kajihara performs the functions of the "memory controller means" for the reasons stated in connection with claim 16.

As to the structure, the only described structure absolutely required to perform the function of "sequentially writing said pixel data to said memory in a first sequence" is address logic having a write signal which can generate one write sequence and the only structure absolutely required to perform the function of "selectively reading said pixel data from said memory in said first sequence . . . or reading said pixel data in a second sequence" is address logic having a

read signal which can generate read addresses for the two different sequences. Appellants do not point out what structure is relied on in figures 10a and 10b. While it would be easy to say that the whole circuit shown in one of figures 10a or 10b is the corresponding structure because Appellants fail to identify any specific structure, we look at the disclosed structure. It appears that the only structure needed to perform the function is a read/write address logic block, e.g., element 1008. Kajihara discloses a read address generator 52 and write address generator 53 (figure 1) to read and write to the page memory 51 in the sequences shown in figures 2A-2D. The description of figure 3 does not show the structure to read and write to the page memory to perform the operations summarized in figure 5, but read and write address generator structure similar to that of figure 1 must exist to scan the page memory as described for the output raster scan mode. We find that the address logic to read and write to the buffer memory in Kajihara is the same as or an equivalent of the structure described because Appellants disclose no more detail of the structure to perform the claimed functions than what is shown in Kajihara.

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Appellants argue (Br17-18):

Lastly, rotation of the image in Kajihara is caused by changing the manner in which data is stored in the page memory. . . . Rotation is thereafter effected when the image data is read out of the page memory in the conventional sequence. Indeed, when propely [sic] understood, it is clear that Kajihara teaches altering the writing sequence of a memory and thus teaches away from the claims.

Regardless of what else is taught by Kajihara, the "output raster scan mode" of Kajihara teaches reading out an image stored in the page memory in accordance with a rotation angle as shown in figures 2A-2D. Thus, Appellants' argument is not persuasive.

For the reasons stated above, the rejection of claim 9 is sustained. Claims 10-12 and 15 are not argued separately and, therefore, fall with claim 9. The rejection of claims 10-12 and 15 is sustained.

Obviousness

Claims 3, 4, 7, and 8

Fujisawa is cited against claims 3 and 4 to show a driving system for driving two different types of displays, such as a cathode ray tube (CRT) and a liquid crystal display (LCD). Fujisawa does not cure the deficiency of Kajihara with

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respect to the rejection of claim 1. Accordingly, the rejection of claims 3 and 4 is reversed.

Okazawa is cited against claims 7 and 8 to show a sequence of repeating sub-sequences of pixel data. Okazawa does not cure the deficiency of Kajihara with respect to the rejection of claim 1. Accordingly, the rejection of claims 7 and 8 is reversed.

Claims 13, 14, 18, and 19

Claims 13 and 14 recite that the read sequence comprises a three bit (claim 13) or six bit (claim 14) read bit sequence for a three bit per pixel (claim 13) or six bit per pixel (claim 14) color display. Claim 18 recites that the first sequence comprises a sequence of repeating sub-sequences, and claim 19, which depends on claim 18, recites that the second sequence is an inverse ordering of the sequence of repeating sub-sequences.

The Examiner finds that Okazawa discloses a sequence of repeating 3.3 sub-sequences of pixel data being used to rotate an image on a video display and concludes that it would have been obvious to incorporate the repeating sub-sequences of pixel data teachings of Okazawa into Kajihara "to provide an

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apparatus for rotating image data in read [sic, real] time with a small capacity memory" (EA4). The Examiner further found with respect to claims 13 and 14 that it is conventional in the art to use three bits per pixel for color flat panel displays (FR4), which finding is not challenged by Appellants.

Appellants argue that Okazawa does not disclose repeating sub-sequences of pixel data or keeping the sub-sequences in the same order regardless of the image rotation so that the three-bit output properly drives red, green, and blue subpixels for a non-rotated as well as rotated image (Br19-21).

The Examiner responds that the claims do not recite keeping the bits of the sub-sequence in order. We agree as to claims 13 and 14 and disagree as to claims 18 and 19.

Okazawa discloses a dot matrix memory where pixels are stored as an $n \times n$ dot unit, e.g., in figure 4A, $n=3$, and "1, 2, 3, 4, 5, 6, 7, 8, and 9" indicates a specific picture element. Okazawa provides hardware to rotate the 3×3 dot unit.

Claims 13 and 14 merely require that a group of bits in the first read sequence is used to represent a pixel. In our opinion, it would have been obvious to one of ordinary skill

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in the art to designate groups of bits in Kajihara as bits for a pixel as recited in claims 13 and 14 in view of Okazawa's disclosure that a group of bits may be used to represent a pixel and the Examiner's finding that it was known in the art to use groups of three and six bits to represent a pixel. Claims 13 and 14 do not recite that the individual read bit sequences must remain the same in the order when the pixel data is read out in a second sequence; compare claim 19. Therefore, the rejection of claims 13 and 14 is sustained.

Claim 19 requires an inverse ordering of the sequence of repeating sub-sequences, which implies that the sub-sequences must be the same for first and second sequences and that the bits which make up the sub-sequences must be kept in the same order. This is not taught by Kajihara which rotates the bits of the image so that groups of bits do not remain in the same order. Okazawa also reverses the order of bits within a 3.3 unit. The Examiner has failed to establish a prima facie case of obviousness with respect to claims 18 and 19. The rejection of claims 18 and 19 is reversed.

Claims 22-24

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Appellants argue that "Fujisawa et al. does not suggest . . . providing a non-rotated image to one display, and a rotated image to a second display" (Br19).

The Examiner concludes that it would have been obvious to use the common display controller of figure 3 of Kajihara to display rotated image data on different types of displays as taught by Fujisawa so that an image can be observed at different angles and perspective (EA5).

We find no motivation in Kajihara or Fujisawa to display different images on two displays. Further, we do not see how the Examiner intends to combine the references to meet the express limitations of claim 22, in particular, the data conversion means which receives the first scanned image data, converts it into second image data and stores it back in memory, creating first and second images in memory. Accordingly, we conclude that the Examiner has failed to establish a prima facie case of obviousness with respect to claim 22. The rejection of claims 22-24 is reversed.

Claims 25 and 26

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Okazawa does not cure the deficiency of Kajihara and Fujisawa with respect to claim 22. Accordingly, the rejection of claims 25 and 26 is reversed.

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CONCLUSION

The rejections of claims 9-17 are sustained.

The rejections of claims 1-4, 7, 8, 18, 19, and 22-26 are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON)	
Administrative	Patent Judge)
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative	Patent Judge)
)	AND
)	INTERFERENCES
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