

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte NOBUAKI MOTOYAMA and SOUICHI KOBAYASHI

Appeal No. 97-1246
Application No. 08/196,731¹

ON BRIEF

Before KRASS, MARTIN, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from a patent examiner's final rejection of claims 1 through 7 and 10. Claims 8 and 9 were objected to as dependent on a rejected claim.

We REVERSE.

¹ Application for patent filed February 15, 1994.

BACKGROUND

The appellants' invention involves detecting and reporting errors in a single-chip microprocessor. The invention detects memory faults by checking the parity of data read from memory (i.e., cache, translation look-aside buffer) built-in to the chip. The invention also detects bus faults by checking the parity of addresses detected during bus snooping. When a memory fault or a bus fault is detected the invention outputs a processor error signal to the outside of the chip to indicate occurrence of the fault. In addition, the invention helps recovery from errors by generating and storing data that identifies specifically errors occurring during access of an external bus.

Claims 1, 4, and 5, which are representative of the invention, follow.

Claim 1. A one-chip microprocessor, comprising:
instruction executing means for executing instructions;
storing means, accessible during instruction execution by said instruction execution means, for storing a plurality of data and parities corresponding to respective data; and

parity generating and checking means, which is connected to said storing means, for, when data is read from said storing means as part of instruction execution of said instruction executing means, comparing the stored parity of the data which has been read, with the parity of the data which has been read to generate a parity error signal when they do not agree;

wherein, when said parity generating and checking means generates said parity error signal, said instruction executing means suspends the instruction execution and outputs a signal to outside the chip to inform of an occurrence of error.

Claim 4. A one-chip microprocessor, comprising:

an instruction execution unit executing instructions;

a cache memory which is accessible during instruction execution by said instruction execution unit;

an internal address bus;

address inputting means for inputting addresses from outside the chip and outputting them to said internal address bus;

address parity inputting means for inputting address parities from outside the chip;

bus snooping means, to which an invalidating request signal of said cache memory is inputted from outside the chip, for snooping said internal address bus and outputting a predetermined signal when an address outputted to said internal address bus is an address to be invalidated; and

parity checking means, which is connected to said internal address bus and said address parity input means, for, when a predetermined signal is outputted from said bus snooping means, checking the address parity outputted to said internal address bus, and generating a parity error signal when detecting a parity error;

wherein, when said parity checking means generates said parity error signal, said instruction execution unit suspends instruction execution and outputs a signal to outside the chip to inform of an occurrence of error.

Claim 5. A one-chip microprocessor, comprising:

an instruction execution unit executing instructions;

a memory which is accessible during instruction execution by said instruction execution unit;

a memory management unit performing address translation by referring to an address translation table of an instruction from said instruction execution unit;

a bus access control unit performing external bus access by request from said instruction execution unit or said memory management unit;

error detecting means for detecting an abnormal bus access generated as a result of bus access by said bus access control unit, and generating different error signals corresponding to kinds of resulting abnormal bus access;

a status register which is connected to said bus access control unit, storing a kind of bus access being executed; and

an error register, which is connected to said error detecting means and said status register, holding error information;

wherein said bus access control unit, when starting the bus access, holds

information indicating whether the bus access is a read access or a write access,

advanced by the examiner, and the evidence of obviousness relied on by the examiner for the rejection. We also have considered the appellants' arguments contained in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal contained in the examiner's answer. After considering the record before us, it is our view that the collective evidence relied on and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention set forth in claims 1-7 and 10. Accordingly, we reverse.

Grouping of the claims

The appellants contend that for the appeal the claims should be considered as four separate groups. (Brief, p. 4) The appellants fail to present arguments, however, why dependent claim 3, which is subject to the same rejection as the independent claim 1, is separately patentable. In the argument section of the appeal brief the appellants make no comment on the dependent claims but argue only the merits of the independent claims. As such, the claims are properly characterized in three groups. The first group comprises

independent claim 1 and claims 2 and 3, both of which depend from claim 1. The second group comprises independent claim 4. The third and last group comprises independent claim 5 and claims 6, 7, and 10, all three of which depend from claim 5. Because the appellants failed to argue separately the patentability of any of the dependent claims, the dependent claims in each of the three groups will stand or fall with their independent claims. See 37 C.F.R. § 1.192(c)(7); M.P.E.P. § 1206; In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

Obviousness

Regarding independent claims 1, 4, and 5, the examiner basically finds that Amini discloses all the claimed limitations except embodying them as a one-chip microprocessor and, upon detection of a parity error, suspending instruction execution and outputting a signal off the chip to indicate occurrence of an error. (Final Rejection, pp. 2-4) Regarding the single-chip embodiment, the examiner concludes that it would have been obvious to integrate Amini's computer system

onto a single chip to reduce the size of the system and reduce power consumption, (Id. at 3), thereby reducing cost.

(Examiner's Answer, p. 9) Based on Amini's teaching that its central processing unit can take whatever action is appropriate upon detection of an error, the examiner concludes that it would have been obvious to suspend execution of instructions. (Final Rejection, p. 3) The examiner also seems to conclude that it would have been obvious to output a signal off the chip to indicate occurrence of an error because the outputting of error signals was well known at the time of the appellant's invention. (Examiner's Answer, p. 5)

Regarding claims 1, 4, and 5, the appellants argue that the examiner failed to show that integration into a single chip would have been obvious at the time of the invention. Regarding claims 1 and 4, the appellants also argue that Amini teaches isolating faulty devices and continuing operation rather than suspending execution of instructions. (Brief, pp. 7-9) The appellants also note that the examiner fails to explain why outputting a signal off the chip would have been necessary. (Id., p. 11-12)

We observe that just because an element was old and well known in an art does not render its combination obvious per se as the examiner's rejection might imply. A suggestion, i.e., a motivation, must be shown for the proposed use of the element.

The suggestion must be based on more than the mere existence of the element. More specifically, the prior art as a whole must have contained something to suggest the "desirability" of using the element to modify a prior art reference. Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick Co., 730 F.2d 1452, 1462, 221 USPQ 481, 488 (Fed. Cir. 1984).

As aforementioned, the examiner explained the desirability of integrating Amini's computer system onto a single chip, viz., reducing the size of the system, reducing power consumption, and reducing cost. (Final Rejection, p. 3; Examiner's Answer, p. 9) In contrast, the examiner failed to identify the desirability of outputting a signal off the chip to indicate occurrence of an error as specified in claims 1 and 4. We agree with the appellants, (Brief, pp. 11-12), that the examiner did not explain why, if the computer system of

Amini were integrated onto a single chip, there would be a need to output a signal off the chip.

Also regarding claim 5, the appellants argue that Amini does not disclose holding information indicating whether an object to be accessed is an instruction or data and information indicating whether a memory management unit accesses an address translation table. (Brief, p. 11) We agree that the Examiner failed to show that Amini discloses these features. The section of Amini cited by the Examiner, (Examiner's Answer, p. 8), as teaching the holding of information indicating whether an object to be accessed is an instruction or data, viz., col. 8, lines 54-68, instead discloses holding an address and time of a parity error. The examiner's allegation that it would have been obvious to store address translation table information in a status register, (Examiner's Answer, pp. 8-9), is irrelevant because it concerns holding translation information rather than information indicating whether a memory management unit accesses an address translation table as claimed. For these

reasons, we do not sustain the rejection of claims 1-7 and 10 under 35 U.S.C. § 103.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-7 and 10 under 35 U.S.C. § 103 is REVERSED.

REVERSED

Errol A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
John C. MARTIN)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
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