

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TONG-CHERN ONG

Appeal No. 1997-2041
Application No. 08/337,131

ON BRIEF

Before HAIRSTON, JERRY SMITH, and FLEMING, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-5, 10 and 11 which represent all of the claims remaining in the application. In

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an Amendment After Final (paper number 15), claim 1 was amended.

In general terms, the invention pertains to the fabrication of electrically programmable read only memory (EPROM) devices. The present invention illustrates a method of making an EPROM device such that a floating gate member asymmetrically overlaps a portion of a buried source region and a buried drain region. The method includes forming a floating gate member such that the floating gate-to-source overlap is shorter than the floating gate-to-drain overlap thus creating a device with shorter erase times and shorter read and programming times. The method further requires that those portions of the floating gate members that form the floating gate-to-source overlap and the floating gate-to-drain overlap are formed subsequent to the formation of the plurality of source and drain regions.

Claim 1 is illustrative of the claimed invention, and
reads as follows:

1. A method of forming an array of electrically erasable non-volatile memory devices on a semiconductor substrate including a monocrystalline silicon layer comprising the steps of:

doping spaced-apart first regions with dopant of a type opposite that of the monocrystalline silicon layer to form a plurality of source areas and a plurality of drain areas, said source areas and said drain areas spaced apart;

growing field oxide areas over the first regions;

growing a tunnel oxide layer between the field oxide areas, the tunnel oxide lying over a plurality of second regions, the second regions lying between the first regions;

forming a plurality of floating gate members, wherein at least a portion of the floating gate members is formed subsequent to the formation of the plurality of source areas and the plurality of drain areas, wherein the portion of the floating gate members formed subsequent to the formation of the plurality of source areas and the plurality of drain areas overlaps a portion of the source areas and a portion of the drain areas thereby forming a floating gate-to-source overlap and a floating gate-to-drain overlap, respectively, wherein the floating gate-to-source overlap is less than the floating gate-to-drain overlap for the portion as formed;

forming an insulating layer over the floating gate members; and

forming a patterned control gate layer.

References¹

¹ Our understanding of the Japanese documents is derived from a reading of the translations prepared for the Patent and Trademark Office. Copies of the translations are attached.

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The prior art relied upon by the examiner as evidence of obviousness are:

Hosokawa (Hosokawa `872)	JP59-229872	Dec. 24, 1984
Hosokawa (Hosokawa `874)	JP59-229874	Dec. 24, 1984
Chen	EP 0,373,698	Jun. 20, 1990

Wolf et al. (Wolf), "Silicon Processing For The VLSI ERA," Vol. 1, Published by Lattice Press, Sunset Beach, California, 1986, pages 1-5. (hereafter Wolf)²

The following three new references applied by this panel of the Board in a new ground of rejection infra are:

Guterman et al. (Guterman)	4,317,273	Mar. 2, 1982
Mazzali	5,028,979	Jul. 2, 1991
Woo	5,147,813	Sep. 15, 1992

(effective filing date Aug. 15, 1990)

Rejections

The following rejections are before us for review;

Claims 1-5, 10 and 11 under 35 U.S.C. § 103 (a) as being unpatentable over Hosokawa (JP59-229872) in view of Chen.

²The examiner relied on Wolf in a new ground of rejection presented in the Examiner's Answer mailed May 29, 1996; however, we note that the examiner failed to list Wolf in the section labeled

"New Prior Art" (section 10) of the Examiner's Answer.

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Claims 1-5, 10 and 11 under 35 U.S.C. § 103 (a) as being unpatentable over Hosokawa (JP59-229874) in view of Chen or Wolf.

Rather than reiterate the examiner's full statement of the above-noted rejections and the conflicting viewpoints advanced by the examiner and appellant regarding those rejections, we make reference to both examiner's answers (Paper Nos. 24 and 26, respectively) for the examiner's reasoning in support of the rejections, and appellant's main brief (Paper No. 23) and reply brief (Paper No. 25) for appellant's arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to appellant's specification and claims, to the applied prior art references³, and to the respective

³In our evaluation of the applied teachings, we have considered all of the disclosure of each teaching for what it would have fairly taught one of ordinary skill in the art. See In re Boe, 355 F.2d 961, 965, 148 USPQ 507, 510 (CCPA 1966). Additionally, this panel of the Board has taken into account

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positions articulated by appellant and the examiner. As a consequence of our review, we have made the determinations which follow.

Appellant has indicated that for purposes of this appeal the claims will all stand or fall together as a single group (Brief, page 4). Consistent with this indication, appellant has made no separate arguments with respect to any of the claims on appeal. Therefore, all the claims before us will stand or fall together. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983). Accordingly, we will only consider the rejection against independent claim 1 as representative of all the claims on appeal in keeping with 37 CFR § 1.192(c)(7).

I. The rejection of claims 1-5, 10 and 11 based upon 35

U.S.C. 103(a)

It is our view, after consideration of the record before us, that the teachings of Hosokawa `872 combined with that of

not only the specific teachings, but also the inferences which one skilled in the art would reasonably have been expected to draw from the disclosure. See In re Preda, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968).

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Chen would not have suggested to one of ordinary skill in the art the obviousness of the invention set forth in claims 1-5, 10 and 11. Accordingly, we reverse.

Our analysis begins with the fact that in rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). We note that to establish the *prima facie* obviousness of a claimed invention, all of the claimed limitations must be taught or suggested by the prior art. See In re Royka, 490 F.2d 981, 984, 180 USPQ 580, 583 (CCPA 1974). Here, the examiner determines (Answer, pages 3 and 4) that the disclosure of Hosokawa `872 teaches all of the features of the claimed invention except the limitations of "forming an array of electrically erasable non-volatile memory devices" and a semiconductor substrate that is formed from "... a monocrystalline silicon layer...."

The examiner takes Official Notice with respect to the limitation of forming an array of electrically erasable non-volatile memory devices.

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In In re Knapp Monarch Co., 296 F.2d 230, 232, 132 USPQ 6,
8 (1961), the court stated that:

Factual matters of which judicial notice is taken can be challenged by production of evidence to the contrary. If therefore, appellant here wishes to challenge the truth of the matters judicially noted by the examiner and the Trademark Trial and Appeal Board, he must challenge it by presenting evidence to the contrary. The record does not show any such evidence. In the absence of such evidence, the board's finding, based on its judicial notice of the facts... is conclusive of the issue here.

Like the examiner (Answer, page 6), we note that the appellant failed to challenge the truth of the matter judicially noted in the rejection (Answer, page 4). Accordingly, this feature is considered admitted prior art by the appellant and accepted as common knowledge in the art of EPROM devices. See In re Lundberg, 244 F.2d 543, 551, 113 USPQ 530, 537 (CCPA 1957); In re Fox, 471 F.2d 1405, 1406-07, 176 USPQ 340, 341 (CCPA 1973).

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The examiner relies on the disclosure of Chen to meet the limitation of a semiconductor substrate including a monocrystalline silicon layer. We note that the appellant did not submit arguments in response to the examiner's reliance on Chen's teaching of a monocrystalline silicon layer for the semiconductor substrate. Instead, as recognized by both the examiner (Answer, page 6) and the appellant (Brief, page 5), this appeal turns on whether or not the prior art relied upon by the examiner discloses the step of:

"... at least a portion of the floating gate members is formed subsequent to the formation of the plurality of source areas and the plurality of drain areas, wherein the portion of the floating gate members formed subsequent to the formation of the plurality of source areas and the plurality of drain areas overlaps a portion of the source areas and a portion of the drain areas..."

The examiner relies heavily on Hosokawa '872 and its teaching that "...the substantial overlap margin (W_1) is required on the drain region side (3) during the formation process...." (Answer, page 7) (emphasis added). From this, the

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examiner reasons that as a result of forming the floating gate, the overlap on the drain region is consequently formed.

In rebuttal, the appellant indicates (Brief, page 5) that Hosokawa `872 fails to explicitly state the order of formation of the source, drain and floating gate. The appellant further submits that the statement pointed to by the examiner is irrelevant to the order of formation of the floating gate relative to the formation of the source and drain regions. We find ourselves in general agreement with the appellant. We fail to find any specific language, nor any intimation whatsoever in the disclosure of Hosokawa `872 that reveals the order in which the floating gate, the source and the drain are formed on the semiconductor substrate. The fact that Hosokawa `872 states that the floating gate region will be stretched across the source region and the drain region and that a substantial overlap margin (W_1) is required on the drain region side (3) during the formation process does not, in itself, shed any light on the order in which the source, the drain and the floating gate are formed on the substrate. Although Hosokawa `872 teaches on page 5, lines 2-6, that the source and drain regions are formed by conventionally-known techniques, the

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examiner has failed to establish that the process of forming the source and drain before the formation of the floating gate represented a conventionally-known technique at the time of the invention by the appellant. Further, the examiner has failed to provide any motivation why one skilled in the art would be driven to form the source and drain prior to the floating gate.

The examiner draws our attention to a certain passage (Answer, page 7) in Hosokawa `872 that states that '*the floating gate region (4) ... are formed in such a way that they will be stretched across the source region (2) and drain region (3) ...*' (Answer page 7)(emphasis added). From this passage, the examiner contends that the implication is that the floating gate is formed subsequent to the source/drain. In response, the appellant asserts (Brief, pages 5 and 6) that the phrase "they will be stretched across the source region (2) and drain region (3)..." represents the future tense and therefore, Hosokawa `872 forms the source and drain regions asymmetrically subsequent to the formation of the floating gate. Here, we are not persuaded by the examiner's or the appellant's arguments.

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We maintain that the disclosure of Hosokawa `872 is completely lacking with respect to setting forth the order of formation of the floating gate and the source/drain regions.

Claims 1-5, 10 and 11 have been further rejected as being unpatentable over Hosokawa `874. This patent is likewise stated by the examiner to meet the step of forming the floating gate subsequent to the formation of the source/drain regions. To the extent of what is disclosed in Hosokawa `874, this patent appears to be no more than cumulative to the disclosure in Hosokawa `872. We find no teaching in Hosokawa `874 of the order of the steps as defined in claims 1-5, 10 and 11, nor do we find any suggestion that this order of steps would produce an unexpected result. We note that the patent to Chen and the teachings of Wolf fail to overcome the deficiencies pointed to in Hosokawa `872 and Hosokawa `874.

II. Secondary Considerations

The appellant's response to the examiner's rejection is twofold. In addition to presenting the arguments addressed above, appellant's rely upon the declaration submitted pursuant to the provisions of **37 CFR § 1.132**. In considering this evidence, we are mindful of our obligation to weigh the entire

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merits of the application and hence consider all the evidence of record. In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788, (Fed. Cir. 1984); In re Rinehardt, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976).

In Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1538, 218 USPQ 871, 879 (Fed. Cir. 1983), the court said:

[E]vidence rising out of the so-called "secondary considerations" must always when present be considered en route to a determination of obviousness. In re Sernaker, *supra*, citing In re Fielder and Underwood, 471 F.2d 640, 176 USPQ 300 (CCPA 1983), see In re Mageli et al., 470 F.2d 1380, 1384, 176 USPQ 305, 307 (CCPA 1973) (evidence bearing on issue of nonobviousness "is never of 'no moment,' is always to be considered and accorded whatever weight it may have.") *Indeed, evidence of secondary considerations may often be the most probative and cogent evidence in the record. It may often establish that an invention appearing to have been obvious in light of the prior art was not. It is to be considered as part of all the evidence, not just when the decisionmaker remains in doubt after reviewing the art.* [Emphasis added.]

With that in mind, we now consider the appellant's arguments and the appellant's declaration in support thereof.

We note that it appears from the record before us that the appellant (Brief, page 4) and the examiner (Answer, page 6)

agree that Hosokawa `872 teaches a non-volatile memory element comprised of a single-cell device. Based on this resolution, the appellant indicates (Brief, page 4) that alignment constraints of single-cell devices suggest the use of self-alignment technology. The appellant points out that self-alignment technology forms the floating gate *prior* to formation of the source/drain regions. (Brief, pages 4, 5 and 7). In support thereof, the declarant, in this case the inventor, proclaims (paragraph 8) that the Hosokawa `872 floating gate is defined first and afterwards the source/drain regions are formed. While we respect the appellant's opinion with respect to the formation of the Hosokawa `872 floating gate, we note that there is no objective evidence offered by the appellant that is supportive of such an opinion. Therefore, we do not find this opinion to be of substantial evidentiary value.

At several points in the Brief and in paragraph 9 of the declaration, the appellant/declarant states that the figure provided as part of the disclosure of Hosokawa `872, in which the floating gate is shown centered between the center points of the two diffusion regions, indicates that the method of formation is most likely a self-alignment process. The

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appellant's argument, strenuously made here, is that the self-alignment process forms the floating gate prior to formation of the diffusion regions.

In rebuttal, the examiner asserts (Answer, page 9) that Hosokawa `872 teaches two embodiments to form the source/drain regions and since only one figure is provided, one embodiment may not be represented by a figure. The examiner insists that the second embodiment in Hosokawa `872 makes it perfectly clear that the source and drain regions are formed before the floating gate (Answer, page 9). In response, the appellant (Reply brief, page 3) correctly notes that the examiner failed to provide any explanation as to why the order of formation is so clear from the referenced passage in Hosokawa `872. The examiner goes on to argue that the relationship of the center of the source/drain with respect to the center of the floating gate fails to disclose anything about the order of processing of the source/drain and floating gate. Based on the totality of evidence in the record surrounding the teachings of Hosokawa `872, we note that there appears to have been a great deal of speculation on the part of both the examiner and the appellant with respect to the teachings of Hosokawa `872 and the order of

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formation of the source/drain regions and the floating gate. However, we will not attempt to speculate as to whether Hosokawa `872 teaches forming the floating gate before or after the source/drain. We simply recognize that neither Hosokawa `872 nor Hosokawa `874 provides adequate disclosures to conclude in what order the floating gate and source/drain regions are formed on the substrate.

The declarant/appellant states in paragraph 10 of the declaration that:

"I am not aware of any single cell device, such as that depicted in Hosokawa, which does not employ a self-aligned process. Non-self-aligned processes are not manufacturable for single cell devices using current semiconductor technology because of alignment problems...." (emphasis added).

The examiner fails to present any arguments to refute the declarant's position that non-self-aligned processes are not manufacturable for single cell devices using current semiconductor technology. Accordingly, absent evidence to the contrary, we are persuaded by the declarant's/appellant's statement in paragraph 10 of the declaration. We have considered the evidence of obviousness and have weighed such evidence of obviousness against the evidence of nonobviousness.

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It is our judgement that, on balance, the evidence of nonobviousness outweighs the evidence of obviousness provided by the examiner. Consequently, we note that: (1) the absence of any teaching in Hosokawa `872 and Hosokawa `874 regarding the order of formation of the source/drain regions; (2) the probative value of the appellant's declaration which must be given fair weight; and (3) the lack of evidence indicating that a single cell can be produced by any other process other than a self-alignment process, all draw us to the conclusion that the appellant's invention defined in claims 1-5, (10, 11)⁴ would not have been obvious under 35 U.S.C. § 103(a) based on Hosokawa `872 combined with Chen or Hosokawa `874 combined with Chen or Wolf. Therefore, both rejections of claims 1-5, 10 and 11 under 35 U.S.C. § 103(a) are reversed.

III. New Ground of Rejection under 37 CFR 1.196(b)

Under the authority of 37 CFR § 1.196(b), this panel of the Board introduces the following new ground of rejection.

Claim 1 is rejected under 35 U.S.C. § 103 as being unpatentable over Mazzali in view of Guterman or Woo.

⁴In claims 10 and 11, it appears that the units of measurement are incorrect. "μ" should be changed to --µm--. This informality should be corrected in any further prosecution that may occur.

The patent to Mazzali (Figures 1 and 3) pertains to a non-volatile buried bit-line EPROM device including a plurality of memory cells. More specifically, there are a plurality of doped spaced apart source and drain areas shown in Figure 3 as elements **2** and **3**, respectively. The grown field oxide areas are represented by elements **5** and **7**. The grown tunnel oxide layer is indicated by elements **4** and **6**. Elements **9** in Figure 3 correspond to the formed floating gate members. The formed insulating layer is represented by element **14** and the formed control gate layer is represented by element **15**, both of which are shown in Figure 3. Thus, Mazzali teaches the claimed invention except for: (1) using a monocrystalline silicon material for the substrate and (2) the step of forming the floating gate members subsequent to forming the plurality of source areas and the plurality of drain areas.

At the outset, we note that the use of a monocrystalline silicon for the material of the substrate represented the state-of-the-art in the buried bit-line EPROM device art at the time of the appellant's invention. This position is further supported by both Guterman and Woo described below.

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The Guterman patent is from the same field of endeavor as the instant application and the patent to Mazzali. The Guterman patent informs us (column 2, lines 36 through 40 and column 3, lines 66 through 68) that, long before the invention by the appellant, in the art of EPROM's, it was known to use a monocrystalline silicon material for the substrate and it was also known to form the source/drain regions prior to the formation of the floating gate layer.

The patent to Woo is also from the same field of endeavor as the instant application and the disclosures of Mazzali and Guterman. Woo teaches (column 4, line 8) that others in the art recognized using monocrystalline silicon for the material of the substrate. Furthermore, Woo suggests (paragraph bridging columns 3 and 4) to the artisan that it is immaterial whether the floating gate layer is formed before or after the source/drain regions.

Thus, applying the test for obviousness⁵ from a combined consideration of the applied teachings, this panel of the Board determines that it would have been obvious to one having

⁵The test for obviousness is what the combined teachings of references would have suggested to one of ordinary skill in the art. See In re Young, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991) and In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981).

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ordinary skill in the art at the time of the invention by the appellant, to modify the EPROM device taught by Mazzali by using the state-of-the-art monocrystalline silicon material for the substrate and by forming the source/drain regions prior to forming the floating gate layer, as taught in column 2 of Guterman and columns 3 and 4 of Woo. In our opinion, the incentive for forming the source/drain regions prior to the formation of the floating gate is explicitly taught in Guterman which teaches that forming the source/drain regions prior to the floating gate layer allows one to use the thick oxide that covers the source/drain region as the mask, rather than relying upon the polysilicon layer as the mask to define the floating gate members. The instructions in the paragraph bridging columns 3 and 4 of Woo guide the artisan to the fact that the order of formation of the floating gate with respect to the formation of the source/drain does not change the resulting structure and that the floating gate could be formed either before or after the source/drain regions. We note that there is no evidence presented by the appellant in the instant record which indicates that the particular order of the steps produces unexpected results or results differing in any way from those

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which would be brought about if another order of steps were followed.

Consequently, it is the opinion of this panel that the cited references considered collectively clearly suggest doing what the appellant in this case has done in claim 1.

In summary, this panel of the Board has:

a) Reversed the rejection of claims 1-5, 10 and 11 under 35 U.S.C. § 103(a) as being unpatentable over Hosokawa (JP59-229872) in view of Chen or Wolf.

b) Reversed the rejection of claims 1-5, 10 and 11 under 35 U.S.C. § 103(a) as being unpatentable over Hosokawa (JP59-229874) in view of Chen or Wolf.

c) Introduced a new ground of rejection of claim 1 pursuant to our authority under 37 CFR § 1.196(b)

The decision of the examiner is reversed.

This decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b) (amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)).

37 CFR

§ 1.196(b) provides that "[a] new ground of rejection shall not be considered final for purposes of judicial review."

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37 CFR § 1.196(b) also provides that the appellant,
WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise
one of the following two options with respect to the new
ground of rejection to avoid termination of proceedings (37
CFR § 1.197(c)) as to the rejected claims:

(1) Submit an appropriate amendment of the
claims so rejected or a showing of facts
relating to the claims so rejected, or both, and
have the matter reconsidered by the examiner, in
which event the application will be remanded to
the examiner . . .

(2) Request that the application be reheard
under 37 CFR § 1.197(b) by the Board of Patent
Appeals and Interferences upon the same record.
. . .

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED 37 CFR 1.196(b)

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JERRY SMITH)	APPEALS
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DECISION: REVERSED; 37 CFR 1.196 (b)
Send Reference(s): Yes No
or Translation (s)
Panel Change: Yes No
Index Sheet-2901 Rejection(s):

Prepared: October 27, 2000

Draft Final

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OB/HD GAU

PALM / ACTS 2 / BOOK
DISK (FOIA) / REPORT