

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte THOMAS F. HEIL,
EDWARD A. MCDONALD,
JAMES M. OTTINGER and
JEFFREY A. HAWKEY

Appeal No.1997-2439
Application 08/417,701¹

ON BRIEF

Before THOMAS, FLEMING, and HECKER, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This a decision on appeal from the final rejection of claims 15 through 19 and 23 through 29.

¹ Application for patent filed April 06, 1994. According to Appellants, this application is a continuation of Application 07/965,033, filed October 22, 1992, now abandoned, which is a continuation of Application 07/761,081, filed September 17, 1991, now abandoned.

Claims 1 through 14 have been canceled. Claims 20 through 22 have been objected to as being dependent upon rejected claims, but the Examiner has indicated that these claims would be allowable if rewritten in independent form including all of the limitations of claims 16 through 19. Appellants have indicated on page 2 of the brief, that they are deferring any action on claims 20 through 22 until after this appeal.

The invention relates to methods and apparatus for interfacing multiple I/O subsystem buses to a common computer system bus.

Independent claim 16 is reproduced as follows:

16. A computer system, comprising:

a system bus;

a processor connected to said system bus;

a first I/O interface circuit connected to said system bus;

a second I/O interface circuit connected to said system bus;

a first I/O bus connected to said first I/O interface circuit, wherein the first I/O bus has a first set of fixed addresses associated with said first I/O bus; and

a second I/O bus connected to said second I/O interface circuit, wherein the second I/O bus has a second set of fixed addresses associated with said second I/O bus, and further wherein the first set of fixed addresses are the same as the second set of fixed addresses,

wherein said first I/O interface circuit includes (1) means for identifying memory addresses and I/O addresses assigned to said first I/O bus by the computer system, and (2) means for translating addresses during accesses to the first set of fixed addresses associated with said first I/O bus from

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memory addresses and I/O addresses assigned to said first I/O bus by the computer system into addresses of the first set of fixed addresses associated with said first I/O bus, and

wherein said second I/O interface circuit includes (1) means for identifying memory addresses and I/O addresses assigned to said second I/O bus by the computer system, and (2) means for translating addresses during accesses to the second set of fixed addresses associated with said second I/O bus from memory addresses and I/O addresses assigned to said second I/O bus by the computer system into addresses of the second set of fixed addresses associated with said second I/O bus.

The Examiner relies on the following references:

Frieder et al. (Frieder)	4,516,199	May 7, 1985
Johnson	4,947,366	Aug. 7, 1990

Claims 15 through 19 and 23 through 29 stand rejected under 35 U.S.C. § 103 as being unpatentable over Frieder in view of Johnson.

Rather than reiterate the arguments of Appellants and the Examiner reference is made to the briefs² and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 15 through 19 and 23 through 29 under 35 U.S.C. § 103.

² Appellants filed an appeal brief on July 25, 1996. Appellants filed a reply brief on December 16, 1996. The Examiner mailed a communication on January 14, 1997 stating that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

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The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), *cert. denied*, 519 U.S. 822 (1996), *citing W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

On pages 7 through 8 of the brief, Appellants argue that Frieder does not disclose either expressly or impliedly, that the I/O bus 102 has a first set of fixed addresses associated with the I/O bus 102, I/O bus 104 has a second set of fixed addresses associated with the I/O bus 104 and the first set of fixed addresses are the same as the second set of fixed addresses. Appellants argue that since Frieder does not disclose the claim limitation that "the first set of fixed addresses are the same as the second set of fixed addresses" the proposed combination of Frieder and Johnson does not arrive at the invention of Appellants' claims.

We note that independent claim 16 recites:

a first I/O bus connected to said first I/O interface circuit, wherein the first I/O bus has a first set of fixed addresses associated with said first I/O bus; and a second I/O bus

connected to said second I/O interface circuit, wherein the second I/O bus has a second set of fixed addresses associated with said second I/O bus, and further wherein the first set of fixed addresses are the same as the second set of fixed addresses; wherein said first I/O bus circuit includes (1) means for identifying memory addresses and I/O addresses assigned to said first I/O bus by the computer system, and (2) means for translating addresses during accesses to the first set of fixed addresses associated with said first I/O bus from memory addresses and I/O addresses assigned to said first I/O bus by the computer system into addresses of the first set of fixed addresses associated with first I/O bus, and wherein said second I/O interface circuit includes (1) means for identifying memory addresses and I/O addresses assigned to said second I/O bus by the computer system, and (2) means for translating addresses during accesses to the second set of fixed addresses associated with said second I/O bus from memory addresses and I/O addresses assigned to said second I/O bus by the computer system into addresses of the second set of fixed addresses associated with said second I/O bus."

We note that independent claim 23 recites a method comprising the steps of:

providing a first I/O bus having a first set of fixed addresses associated therewith; providing a second I/O bus having a second set of fixed addresses associated therewith, wherein the first set of fixed addresses are the same as the second set of fixed addresses . . . translating addresses during accesses to the first set of fixed addresses associated with the first I/O bus or the second set of fixed addresses associated with the second I/O bus from memory addresses and I/O addresses assigned to the first I/O bus or the second I/O bus by the computer system into a addresses of the first set of fixed addresses associated with the first I/O bus or the second set of fixed addresses associated with the second I/O bus."

We note that independent claim 29 recites a method which has similar method steps as recited in Appellants' claim 23.

On page 5 of the answer, the Examiner argues that Frieder's addresses of each device is inherently the same when it is accessed via the first I/O bus as when it is accessed via the second I/O

bus. The Examiner further argues that the assignment and use of memory addresses and I/O addresses is inherent to the operation of the computer system. On page 6 of the answer, the Examiner states that Frieder does not disclose that the first I/O interface circuit includes means for translating addresses during accesses to the first addresses assigned to the first I/O bus by the computer system from the memory and I/O addresses assigned to said first I/O bus by the computer into the addresses of the first set of fixed addresses associated with said second I/O bus and that the second I/O interface circuit includes means for translating addresses during accesses to the second set of addresses assigned to said second I/O bus by the computer system from memory and I/O addresses assigned to said second I/O bus by the computer system into addresses of the second set of fixed addresses associated with said second I/O bus. The Examiner argues that Johnson discloses means for translating these addresses and that it would be obvious to employ the Johnson translators into the Frieder's system.

On pages 4 and 5 of the reply brief, Appellants pointed out that if the Frieder's set of addresses associated with the first bus is equivalent to a first set of fixed addresses and the Frieder's set of addresses associated with the second bus is equivalent to a second set of fixed addresses then the two sets of addresses would not be the same. Appellants argue that if they were the same, the computer system as disclosed by Frieder could not properly operate, since the computer system does not include an identifying means or a translating means to be able to distinguish between the two sets of addresses.

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Upon our review of Frieder, we fail to find that Frieder teaches a translating means or identifying means. Furthermore, we fail to find that Frieder teaches that the addresses associated with the I/O bus 102 and the addresses associated with the I/O bus 104 are the same. We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a *prima facie* case. *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984); *In re Knapp-Monarch Co.*, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); *In re Cofer*, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Our reviewing court states in *In re Piasecki*, 745 F.2d at 1472, 223 USPQ at 788 the following:

The Supreme Court in *Graham v. John Deere Co.*, 383 U.S. 1 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under Section 103. As adapted to ex parte procedure, Graham is interpreted as continuing to

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place the "burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under section 102 and 103". *Citing In re Warner*, 379 F.2d 1011, 1020, 154 USPQ 173, 177 (CCPA 1967).

Furthermore, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by person of ordinary skill.'" *In re Robertson*, slip Op 98-1270 (Fed. Cir. February 25, 1999), *citing Continental Can Co v. Monsanto Co.*, 948 F.3d 1264, 1268, 20 USPQ2d 1756, 1749 (Fed. Cir. 1991). "Inherency, however, may be established by probabilities or possibilities. The mere fact that a certain thing may result for a given set of circumstances is not sufficient." *Id. citing Continental Can Co. v. Monsanto Co.*, 948 F.3d 1264, 1269, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

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In view of the foregoing, we have not sustained the rejection of claims 15 through 19 and 23 through 29 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JAMES D. THOMAS)
Administrative Patent Judge)
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)
) BOARD OF PATENT
MICHAEL R. FLEMING)
Administrative Patent Judge) APPEALS AND
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) INTERFERENCES
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