

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHIH-SIUNG WU

Appeal No. 97-2630
Application 08/186,050¹

ON BRIEF

Before SCHAFER, LEE, and TORCZON, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1, 13 and 15. Claims 2-6, 9, 14, 17 and 18 have been canceled. Claims 20-34 have been withdrawn from consideration. Claims 7, 8, 10, 11, 12, 16 and 19 have not been indicated as allowable, but the rejection of these claims also has not been maintained in the examiner's answer.

References relied on by the Examiner

¹ Application for patent filed January 24, 1994.

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Duschatko et al. (Duschatko) 1992	5,146,461	Sep. 08,
Hurst et al. (Hurst)	4,870,530	Sep. 26, 1989
Chua 1990	4,891,683	Jan. 02,
Rogers	5,049,763	Sep. 17, 1991
Schanin et al. (Schanin) 1991	5,067,071	Nov. 19,
Kimura et al. (Kimura)	5,323,043	Jun. 21, 1994
Fujita et al. (Fujita)	5,336,915	Aug. 09, 1994
Pianka	5,345,357	Sep. 06, 1994
Sundby	5,371,419	Dec. 06, 1994
Partovi et al. (Partovi)	5,453,713	Sep. 26,
1995		

The Rejection on Appeal

In the final Office action, claims 1, 7, 8, 10-13, 15, 16 and 19 were rejected under 35 U.S.C. § 103 as being unpatentable over Duschatko. (Paper No. 10).²

The appeal brief identified the issue on appeal as the rejection of claims 1, 7, 8, 10-13, 15, 16, and 19 under 35 U.S.C. § 103 over Duschatko. The appellant grouped claims 10-12 with claim 1, and claims 7, 8, 16 and 19 with claim 15.

² In the final Office action, claims 1, 7, 8, 10-13, 15, 16 and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated by a certain prior art reference. This rejection, however, was withdrawn in an advisory Office action dated September 16, 1996. (Paper No. 14).

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The examiner's answer maintained only the rejection of claims 1, 13 and 15. See examiner's answer at page 6. While in all likelihood the examiner did not intend to withdraw the rejection of claims 7, 8, 10-13, 15, 16, and 19, he did not include them in the statement of rejection within the examiner's answer. We recognize that the appellant has grouped claims 10-12 with claim 1 and claims 7, 8, 16 and 19 with claim 15, but grouping of claims does not operate to cancel claims. The examiner still must maintain those rejections which he deems proper to apply. The rejection of claims is too important to be left to likelihoods and probabilities. Doing that would promote uncertainty and also trivialize the seriousness of statements made on the written record.

Accordingly, the rejection of claims 7, 8, 10-12, 16 and 19 is considered as withdrawn and the only claims rejected are claims 1, 13 and 15.

The Invention

The invention is directed to an integrated circuit. Claim 13 depends from claim 1. Independent claims 1 and 15 are reproduced below:

1. An apparatus comprising a SCSI controller and an Ethernet controller integrated onto a single integrated circuit chip, wherein the SCSI and Ethernet controller include digital control circuitry coupled to buffers, and the Ethernet controller includes analog circuitry, wherein circuitry on the integrated circuit chip is configured to limit noise generated in the analog circuitry by signals in the digital control circuitry.

15. An integrated circuit comprising:
internal circuitry;

buffers; and

V_{ss} leads including a first set of V_{ss} leads connected to the internal circuitry and a second set of V_{ss} leads connected only to the buffers.

Opinion

We sustain the rejection of claim 1. Our affirmance of the obviousness rejection is based only on the arguments presented by appellants in their brief. Arguments not raised in the brief are not before us, are not at issue, and thus are considered as waived.

The rejection of claims 13 and 15 cannot be sustained. A reversal of the rejection on appeal should not be construed as an affirmative indication that the appellants' claims are patentable over prior art. We address only the positions and

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rationale as set forth by the examiner and on which the examiner's rejection of the claims on appeal is based.

As per claim 1, the appellant states (Brief at page 2):

Appellant's invention is an integration of components of a SCSI controller and an Ethernet controller onto a single chip with circuitry configured to reduce noise generated by digital signals so that the analog circuitry will operate within an acceptable error margin. High current in the digital SCSI controller circuitry has previously prevented manufacturers from integrating SCSI and Ethernet controllers due to unacceptable errors created in the analog Ethernet components. (Page 2, lines 16-34).

The appellant's specification explains that with the presence of sensitive analog components in the Ethernet controller, such as the phase lock loop, noise generated from digital signals from SCSI components has prevented manufacturers from integrating SCSI and Ethernet components together. See specification at page 2.

Duschatko does not disclose integrating an SCSI controller and an Ethernet controller together on a single integrated circuit chip as is required by claim 1. The appellant acknowledges that combining analog and digital circuits onto one integrated circuit chip is generally within the knowledge of one with ordinary skill in the art, as is

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indicated by the examiner. According to the appellant, however (Brief at pages 4-5), (1) simply combining SCSI controller and Ethernet controller onto a single integrated circuit chip will not create a device functioning within an acceptable error margin, (2) taking standard steps to isolate analog and digital components on an integrated Ethernet and SCSI controller will not reduce errors in the analog circuitry below an acceptable margin , and (3) including additional noise reduction circuitry, as further claimed in claim 1, necessary to reduce noise within an acceptable error margin, is not disclosed by Duschatko and is not within the knowledge of one with ordinary skill in the art.

The appellant's arguments are not commensurate in scope with the features recited in claim 1. Claim 1 is broader in scope and does not support the arguments on which the appellant relies. For instance, insofar as noise reduction is concerned, claim 1 simply recites that "circuitry on the integrated circuit chip is configured to limit noise generated in the analog circuitry by signals in the digital control circuitry." Claim 1 does not require that digital noise be sufficiently reduced such that the analog circuitry in the

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Ethernet controller can operate within an acceptable error margin. All that must happen is that noise caused by digital circuitry be limited. Accordingly, any reduction in the digital noise, including that made possible by what the appellant has referred to as "standard steps" (Brief at page 5) for isolating analog and digital components, is sufficient to meet the claim. While the resulting structure may not be as reliable as one made according to additional steps taken to further reduce the digital noise, it cannot be said that the resulting device is either unfunctional or without utility. The law does not require commercial grade performance in all devices properly deemed obvious over the prior art. All of the teachings of the prior art, including nonpreferred embodiments, are relevant. See, e.g., In re Lamberti, 545 F.2d 747, 750, 192 USPQ 278, 280 (CCPA 1976). It is evident that the appellant should have inserted into claim 1 a specific error margin that must not be exceeded, but that the appellant has not done.

The appellant has acknowledged and referred to "standard steps" for noise reduction, and the examiner has found that certain noise reduction techniques on integrated circuit chips

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were well known to one with ordinary skill in the art and would have been readily applied by one with ordinary skill in the art when integrating analog and digital circuits together. For support, the examiner cited to Partovi, Sundby, Roger, Fujita, and Kimura (Examiner's Answer at pages 5-6). We agree with the examiner that a standard digital noise reduction technique for integrated circuit chips or a digital noise reduction technique that would have been well known to one with ordinary skill in the art would be sufficient to meet the claimed feature "to limit noise generated in the analog circuitry by signals in the digital control circuitry."

On pages 5-6 of the appeal brief, the appellant argues:

For a person of ordinary skill in the art to integrate SCSI and Ethernet controllers on a chip, the person would need to realize that circuitry should be configured to isolate analog and digital components as well as to reduce the effect of a 48 milliamp input signal as done by separating V_{ss} lines for buffers (Appellant's specification page 9, line 19 through page 11, line 10) and configuring buffers to switch current in delayed steps (Appellant's specification page 11, line 11 through page 18, line 4), and by isolating the power supplies (Appellant's specification page 22, line 11 through page 25, line 23).

As we have already noted above, the arguments of the appellant are not commensurate in scope with what has been recited in

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claim 1. Claim 1 does not recite anything regarding the separation of V_{ss} lines for buffers or the isolation of power supplies.

For the foregoing reasons, the rejection of claim 1 as being unpatentable over Duschatko is sustained.

Claim 15 recites an integrated circuit comprising internal circuitry, buffers, and a first set of V_{ss} leads connected to the internal circuitry and a second set of V_{ss} leads connected only to the buffers. In light of the appellant's specification (see for example pages 1-3), it is understood that "buffers" means output buffers. Also, evidently according to the appellant, "internal circuitry" means the remaining circuitry on the integrated circuit chip other than the buffers. (See Reply Brief at page 3, lines 19-20). The examiner states that Duschatko does not disclose separate V_{ss} connections as claimed but that such a limitation would have been obvious based on well-known design guidelines. The evidence the examiner provided in support of his finding of well-known design guidelines, however, does not support the obviousness conclusion. The examiner cited Fujita as teaching separate V_{ss} ground connection limitations, without a

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meaningful explanation. (Examiner's Answer at page 5). It is not known what in Fujita the examiner regards as separate V_{ss} leads to the internal circuitry and to buffers.

As is defined in appellant's specification, V_{ss} means general digital ground. (Specification at page 9). While the portion of Fujita cited by the examiner teaches making separate ground connections to digital and analog circuits on an integrated circuit chip (column 6, line 63 to column 7, line 8), it is not seen how that would have suggested one set of ground leads exclusively for output buffers as is required by claim 15. The examiner has not pointed to any disclosure or suggestion of an integrated circuit chip containing both digital and analog circuits and the only digital circuits of which are comprised of output buffers. That teaching would have been necessary to combine with what Fujita shows to arrive at the appellant's claimed invention. Even if the prior art may be modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992).

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For the foregoing reasons, the rejection of claim 15 cannot be sustained.

Claim 13 depends from claim 1 and specifically requires three separate power distribution networks for (1) the analog circuitry, (2) the digital control circuitry, and (3) the buffers. Additionally, claim 13 requires silicon control rectifiers to be connected between the power distribution networks, for sensing when a voltage difference between two networks exceeds a predefined limit, and for forming a conductive path between the two networks when the predefined limit is reached.

At page 5 of the answer, the examiner stated that silicon control rectifiers are commonly used and cited to Chua. At page 4 of the answer, the examiner stated that silicon control rectifiers are commonly used between the internal circuit portion and pins and cited to Hurst. At page 5 of the answer, the examiner stated that Fujita teaches separately supplying power. In discussing the rejection of claim 13, the examiner stated (answer at page 7):

As can be seen from above demonstration of the prior art sections, distributing a power or using SCRs to protect the integrated circuit portions are no more than one of the most typical or fundamental

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design consideration/criteria in the art. Of course, in order to combine a digital and analog circuits into a single chip, the designer must consider **standard/well known design guidelines** like the noise or transient/static discharge preventions. The problems such as the noise and transient/static discharge are one of the most typical or fundamental consideration when it comes to design or integrate a combined digital-analog circuits.

It would have been obvious at the time the invention was made to one having ordinary skill in the art to combined the functional circuits of the Duschatko according to the designer's choice for the reasons discussed above. [Emphasis in original.]

The examiner's reasoning is directed to generalities rather than the specific features recited in claim 13. For instance, while silicon control rectifiers may have been well known, that does not mean it was well known to use them in the specific arrangement required by appellant's claim 13. Fujita teaches separate power supply lines for digital and analog circuits on an integrated circuit chip, not three separate power distribution networks, one for analog circuitry, another one for digital control circuitry, and still another one for buffers. Also, Hurst's using silicon controlled rectifiers between circuit portions 16, 18, and 20, and pins P1-Pn is not the same as connecting silicon control rectifiers between separate power distribution networks, where each silicon

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control rectifier senses when a voltage difference between two of the power distribution networks exceed a predefined limit, and forms a conductive path between the two networks when the predefined limit is reached, as is recited in claim 13.

While it may be true that one with ordinary skill in the art would consider standard and well known design guidelines when integrating digital and analog circuits on a chip, the examiner has provided no factual evidence to establish that after such consideration one with ordinary skill in the art would have arrived at the appellant's claimed invention. The record does not establish either (1) that it was well known to use one power distribution network for buffers, one for analog circuitry, and one for digital control circuitry, or (2) that it was well known to use silicon control rectifiers to connect these power distribution networks such that each silicon control rectifier can sense when a voltage difference between two networks exceeds a predetermined limit and then form a conductive path when the predefined limit is reached. The examiner has failed to establish a prima facie case that the claimed invention would have been obvious to one with ordinary skill in the art in light of Duschatko and that

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