

**THIS OPINION WAS NOT WRITTEN FOR PUBLICATION**

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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**Ex parte** HIDEKI TAKAHASHI,  
HIDENORI NISHIHARA,  
MASANA HARADA and  
TADAHARU MINATO

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Appeal No. 1997-2846  
Application 08/388,599<sup>1</sup>

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HEARD: JANUARY 11, 2000

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Before Hairston, Hecker and Lall, **Administrative Patent  
Judges.**

HECKER, **Administrative Patent Judge.**

**DECISION ON APPEAL**

This is a decision on appeal from the final rejection of  
claim 7. Claims 3 through 6, 8, 10 through 12 and 18 through

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<sup>1</sup> Application for patent filed February 14, 1995.

20 have been allowed<sup>2</sup>. Claims 14 through 17 have been withdrawn from consideration as being directed to a non elected invention. Claims 9 and 13 have been canceled.

Appellants' invention relates to an insulated gate semiconductor device having a trench gate. In particular, looking at Figure 1, the semiconductor device 151 includes a first semiconductor layer 204, a second semiconductor layer 205, and a third semiconductor layer 206. Trenches 207 are arranged substantially in a striped form along the upper surface and formed from the upper surface to the first semiconductor layer 204. Each trench 207 includes a gate insulating film 209 and a gate electrode 210. The second semiconductor layer 205 and the third semiconductor layer 206 are selectively exposed in the upper main surface interposed between adjacent trenches 207. Looking at Figure 11, a maximum distance  $L_{max}$  is shown.  $L_{max}$  is determined by the formula  $V_{pn} > m \times J_{pr} \times D_{pn} \times L_{max}$ , where  $V_{pn}$  is a built-in potential peculiar to a function portion of the second semiconductor layer 205 and the third semiconductor layer 206,

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<sup>2</sup> Note the Advisory Action, Paper No. 14, mailed June 4, 1996.

$J_{pr}$  is the density of current flowing in the second semiconductor layer 205 right under the third semiconductor layer 206 when a main current with a magnitude corresponding to a rated current of the device is passed through the device,  $m$  is a ratio of the predetermined limit current value and the rated current, and  $D_{pn}$  is the resistivity of the second semiconductor layer 205 right under the third semiconductor layer 206. Thus, a bias voltage occurring at a junction portion between the second semiconductor layer and the third semiconductor layer does not exceed the built-in potential  $V_{pn}$  when the main current with the magnitude corresponding to the rated current is caused to flow in the device and will not cause conduction of a parasitic transistor.

Independent claim 7 is reproduced as follows:

7. An insulated gate semiconductor device, comprising  
a semiconductor base body having an upper main surface  
and a lower main surface,  
the semiconductor base body comprising,  
a first semiconductor layer of a first conductivity type,  
a second semiconductor layer of a second conductivity  
type provided on the first semiconductor layer, and

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a third semiconductor layer of the first conductivity type selectively formed in an upper surface portion of the second semiconductor layer,

said semiconductor base body having a plurality of trenches arranged substantially in a stripe form along said upper main surface and formed from said upper main surface to said first semiconductor layer,

said trench having a gate insulating film formed covering its inner wall and a gate electrode buried in said trench with the gate insulating film interposed therebetween,

said second semiconductor layer and said third semiconductor layer being selectivity exposed in said upper main surface interposed between adjacent said trenches,

said insulated gate semiconductor device further comprising,

a first main electrode electrically connected to both of said second and third semiconductor layers on said upper main surface and insulated from said gate electrode,

a second main electrode electrically connected to said lower main surface, and

overcurrent protection means for limiting the magnitude of main current flowing between said first main electrode and said second main electrode so as not to exceed a predetermined limit current value, and

shape of said third semiconductor layer being set so that a maximum distance  $L_{max}$  defined as a distance to a point which is farthest from an exposure surface of said second semiconductor layer in said upper main surface among points on an intersection of a boundary plane of said third semiconductor layer and said second semiconductor layer and said trench is given by  $V_{pn} > m \times J_{pr} \times P_{pn} \times L_{max}$  for built-in potential  $V_{pn}$  peculiar to a junction

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portion of said second semiconductor layer and said third semiconductor layer, density  $J_{pr}$  of current flowing in said second semiconductor layer right under said third semiconductor layer when main current with magnitude corresponding to rated current of the device is passed between said first main electrode and said second main electrode, a ratio  $m$  of said predetermined limit current value and said rated current, and resistivity  $P_{pn}$  of said second semiconductor layer right under said third semiconductor layer.

The reference relied on by the Examiner is as follows:

Temple                    EP 0 159,663 A2                    Oct. 30, 1985

Claim 7 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Temple.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the brief, reply brief and the answer for the respective details thereof.

#### **OPINION**

After a careful review of the evidence before us, we disagree with the Examiner that claim 7 is anticipated under 35 U.S.C. § 102(b) by Temple.

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. **See *In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and ***Lindemann***

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**Maschinenfabrik GMBH v. American Hoist & Derrick Co.**, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). "Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." **RCA Corp. v.**

**Applied Digital Data Sys., Inc.**,

730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984), cert. dismissed, 468 U.S. 1228 (1984), citing **Kalman v. Kimberly-**

**Clark Corp.**, 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983). The Examiner, in the Answer, explains how Temple

meets all the limitations of claim 7 except for the last paragraph of claim 7 where Lmax is recited. At page 9 of the Answer the Examiner states:

Although Temple does not explicitly propose a sophisticated mathematical formula to explain the relationship among different electrical parameters of the structure [including Lmax], Temple has accomplished a high maximum lateral drop and latching current density to avoid latching on the parasitic transistor which is the **same goal** of appellants' disclosed and claimed invention. Therefore, no **prima facie** case of obviousness is needed to be established by the examiner and the appellants have not proved that the structure of Temple [ ] cannot anticipate[] and/or inherently have the claimed relationship among different

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electrical parameters of alike structures to accomplish the same prevention of incurring conduction of the parasitic transistor. (Emphasis added.)

Although we agree with the Examiner that Temple teaches all the claim limitations except  $L_{max}$  in the last paragraph, we cannot agree with the Examiner's above statement for several reasons. Even if Temple accomplishes the same goal as Appellants, this is not evidence of anticipation unless the goal is accomplished with the same structure claimed. Also, Appellants are not required to show that Temple "cannot anticipate[] and/or inherently have the claimed relationship." The Examiner must show anticipation and/or inherency, and Appellants must counter the Examiner's evidence.

The Examiner has indicated how Temple achieves the same result (Answer-bottom of page 8), but this does not involve Appellants'  $L_{max}$ , or anything equivalent thereto. Temple minimizes the lateral length of current path 52. At page 17 of Temple, parameters similar to those used by Appellants, are used to determine path 52. **But, path 52 is not  $L_{max}$  as**

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**defined by Appellants.** Even if path 52 achieves the same electrical result, actually or inherently, path 52 is not the same as Lmax, and the Examiner has not shown that minimizing path 52 will result in Appellants' defined maximum distance of Lmax.

The Examiner **has not shown** that Temple's structure, using similar parameters to determine path 52, inherently results in a structure defined by Appellants' claim 7 using Lmax. In the absence of such a showing by the Examiner, it is not Appellants' burden to show how Temple **does not inherently result** in their claimed structure.

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In view of the foregoing, the decision of the Examiner  
rejecting claim 7 under 35 U.S.C. § 102 is reversed.

**REVERSED**

Kenneth W. Hairston	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
Stuart N. Hecker	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
	)	
)		
Parshotam S. Lall	)	
Administrative Patent Judge	)	

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