

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 59

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TAKUJI YOSHIDA

Appeal No. 1997-3161
Application 08/450,553

HEARD: FEBRUARY 10, 2000

Before HAIRSTON, RUGGIERO and HECKER, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 6-9, 43, 45, 46, and 50-57. Claims 1-5, 10-42, 44, and 47 through 49 were canceled earlier in the prosecution. An amendment after final rejection filed July 16, 1996 which canceled claim 50 was entered by the Examiner. Accordingly,

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claims 6-9, 43, 45, 46, and 51-57 are before us on appeal.

The claimed invention relates to a method of erasing the memory cells of an electrically erasable programmable read-only memory, commonly referred to as an EEPROM. More particularly, Appellant indicates at pages 8 through 10 of the specification that a first voltage higher than both the supply voltage and the ground voltage and a second voltage lower than both the supply voltage and ground are generated. During the erasing operation, the first generated voltage is applied to the control gate of a nonvolatile storage transistor of a memory cell, while the second voltage is applied to either the source or the drain.

Claim 43 is illustrative of the invention and reads as follows:

43. A method of erasing an EEPROM memory cell supplied with a supply voltage and a ground voltage, the EEPROM memory cell comprising a storage transistor including a substrate having a first conductivity type and provided therein with a source and a drain each of a second conductivity type, a floating gate disposed over the substrate and a control gate disposed over the floating gate, said method comprising steps of:

applying a first voltage higher than both the supply voltage and the ground voltage to the control gate; and

applying, at least partially concurrently with the application of the first voltage, a second voltage lower than both the supply voltage and the ground voltage to at

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least one of the source and drain, whereby electrons are injected into the floating gate when both the first and second voltages are applied.

The Examiner relies on the following prior art:¹

McElroy 1985	4,503,524	Mar. 05,
Anderson et al. (Anderson) 1990	4,953,928	Sep. 04,
Terasawa et al. (Terasawa) 1991	5,022,000	Jun. 04,
		(Filed Sep. 06, 1989)
Gill et al. (Gill) 1991	5,047,981	Sep. 10,
		(Filed Jun. 30, 1989)
Haddad et al. (Haddad) 1991	5,077,691	Dec. 31,
		(Filed Oct. 23, 1989)
Santin 1992	5,122,985	Jun. 16,
		(Filed Apr. 16, 1990)
Gill et al. (Gill) 1992	5,134,449	Jul. 28,
		(Filed Feb. 26, 1991)
D'Arrigo et al. (D'Arrigo) 1992	5,168,335	Dec. 01,
		(Filed Aug. 06, 1991)
McElroy et al (McElroy) 1993	5,177,705	Jan. 05,
		(Filed Sep. 05, 1989)
Gill et al. (Gill) 1993	5,187,683	Feb. 16,
		(Filed Aug. 31, 1990)
D'Arrigo et al. (D'Arrigo)	5,265,052	Nov. 23,

¹ With the exception of Haddad and Anderson, the listed references were not applied in the prior art rejection but, rather, only cited as evidence in support for the Examiner's position as to Appellant's alleged unconventional usage of the term "erase."

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1993
1989) (Effectively Filed Jul. 20,
Caywood 5,235,544 Aug. 10,
1993
(Filed Nov. 09, 1990)

Anantha et al. (Anantha), "Electrically Erasable Floating Gate Field Effect Transistor Memory Cell," 17 IBM Technical Disclosure Bulletin, no. 8, 2311-13 (January 1975).

Dockerty, "Nonvolatile Memory Array with Single FAMOS Device Per Cell," 17 IBM Technical Disclosure Bulletin, no. 8, 2314-15 (January 1975).

Kikuchi et al. (Kikuchi), "A 2048-Bit N-Channel Fully Decoded Electrically Writable/Erasable Nonvolatile Read Only Memory," 1st European Solid-State Circuits Conference (ESSIRC), Kent, England, 66-7 (September 1975).

Claims 6-9, 43, 45, 46, and 51-57 stand finally rejected under the "enabling" clause of the first paragraph of 35 U.S.C.

§ 112, as well as under the second paragraph of 35 U.S.C.

§ 112 for failure to particularly point out and distinctly claim the invention. Claims 6-9, 43, 45, 46, and 51-57 stand further finally rejected under 35 U.S.C. § 103 as being unpatentable over Haddad in view of Anderson.

Rather than reiterate the arguments of Appellant

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and the Examiner, reference is made to the Briefs² and Answers for the respective details thereof.

It is our view, after consideration of the record before us, that Appellant's specification in this application provides an enabling disclosure in a manner which complies with the requirements of 35 U.S.C. § 112. We are also of the view that the appealed claims particularly point out the invention in a manner which complies with 35 U.S.C. § 112, second paragraph. Finally, it is our opinion that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention

² The Appeal Brief was filed September 13, 1996. In response to the Examiner's Answer dated April 7, 1997, a Reply Brief was filed June 6, 1997 which was acknowledged and entered by the Examiner without further comment on October 16, 1997.

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as set forth in claims 6-9, 43, 45, 46, and 51-57.

Accordingly, we reverse.

We consider first the rejection of claims 6-9, 43, 45, 46, and 51-57 for lack of enablement under the first paragraph of 35 U.S.C. § 112. In order to comply with the enablement provision of 35 U.S.C. § 112, first paragraph, the disclosure must adequately describe the claimed invention so that the artisan could practice it without undue experimentation. In re Scarbrough, 500 F.2d 560, 566, 182 USPQ 298, 303 (CCPA 1974); In re Brandstadter, 484 F.2d 1395, 1404, 179 USPQ 286, 293 (CCPA 1973); and In re Gay, 309 F.2d 769, 774, 135 USPQ 311, 316 (CCPA 1962). If the Examiner has a reasonable basis for questioning the sufficiency of the disclosure, the burden shifts to Appellant to come forward with evidence to rebut this challenge. In re Doyle, 482 F.2d 1385, 1392, 179 USPQ 227, 232 (CCPA 1973), cert. denied, 416 U.S. 935 (1974); In re Brown, 477 F.2d 946, 950, 177 USPQ 691, 694 (CCPA 1973); and In re Ghiron, 442 F.2d 985, 992, 169 USPQ 723, 728 (CCPA 1971). However, the burden is initially upon the Examiner to establish a reasonable basis

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for questioning the adequacy of the disclosure. In re Strahilevitz, 668 F.2d 1229, 1232, 212 USPQ 561, 563 (CCPA 1982); In re Angstadt, 537 F.2d 498, 504, 190 USPQ 214, 219 (CCPA 1976); and

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In re Armbruster, 512 F.2d 676, 677, 185 USPQ 152, 153 (CCPA 1975).

The Examiner asserts (Answer, pages 5 and 6) that, since the conductivity types of the substrate and the source/drain are not recited in the claims, there are combinations of conductivity types for which the invention would be inoperative, i.e. electrons would not be transported to the floating gate. After careful review of the arguments of record, we are in agreement with Appellant's stated position in the Briefs. As pointed out by Appellant, the disclosure in the specification relative to Figure 3 of the drawings describes a detailed embodiment of the invention, the operativeness of which the Examiner has not questioned, which includes an indication of the conductivity types of the semiconductor components of the memory cell. In our view, the present disclosure is of sufficient detail so as to enable one of ordinary skill to select the proper combination of conductivity types to enable an operative embodiment of the claimed invention.

In view of the above, we find that the Examiner has not established a reasonable basis for challenging the sufficiency

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of the instant disclosure. While some experimentation by artisans may be necessary in order to practice the invention, we find that such experimentation would not be undue. Accordingly, we will not sustain the rejection of claims 6-9, 43, 45, 46, and 51-57 under the first paragraph of 35 U.S.C. § 112.

We now turn to a consideration of the Examiner's rejection of claims 6-9, 43, 45, 46, and 51-57 under 35 U.S.C. § 112, second paragraph. The general rule is that a claim must set out and circumscribe a particular area with a reasonable degree of precision and particularity when read in light of the disclosure as it would be by the artisan. In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971). Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed in light of the specification. Seattle Box Co. v. Industrial Crating & Packing, Inc., 731 F.2d 818, 826, 221 USPQ 568, 574 (Fed. Cir. 1984).

It is noted, initially, that the Examiner's rationale in making this rejection is linked to the rationale relied on in making the lack of enablement rejection discussed supra. In

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the Examiner's view (Answer, pages 5 and 6), since the claims merely recite a particular voltage biasing without reciting the conductivity types of the substrate and source/drain regions, the claimed function of "erasing" is indeterminate. In a related argument, the Examiner questions Appellant's use of the term "erase" to categorize the injection of electrons into the floating gate, alleging that such terminology is contrary to conventional usage in which "erase" would signify the removal of electrons from the floating gate.

After reviewing the arguments of record, we are in agreement with Appellant that no ambiguity or lack of clarity exists in the claim language. As we alluded to in our discussion concerning the lack of enablement rejection, the designation of the particular conductivity types of the various semiconductor regions in the claims is not necessary for an understanding of the metes and bounds of the invention. With respect to the Examiner's concern with Appellant's allegedly unconventional usage of the term "erase", we note that, in addition to the clear definition of the term supplied by Appellant at page 8 of the specification, several of the references cited by the Examiner in support of his position

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(i.e. Dockerty and Anantha) in fact use Appellant's definition. For the above reasons, it is our view that the skilled artisan, having considered the specification in its entirety, would have no difficulty ascertaining the scope of the invention recited in the claims on appeal. Therefore, the rejection of independent claims 43 and 51, and claims 6-9, 45, 46, and 52-57 dependent thereon, under the second paragraph of 35 U.S.C. § 112 is not sustained.

Turning to a consideration of the obviousness rejection of the appealed claims, we note that in rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1,17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication

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in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

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With respect to independent claims 43 and 51, the Examiner, as the basis for the obviousness rejection, proposes to modify the programming operation (equivalent to Appellant's erasing operation) in the EEPROM cell array of Haddad by relying on Anderson to provide a teaching of applying a negative potential to the source region in Haddad. In the Examiner's view (Answer, page 7), the skilled artisan would have been motivated to forward bias the source region in Haddad to enhance the flow of electrons into the floating gate in view of the teachings of Anderson.

In response, Appellant asserts that the Examiner has failed to set forth a prima facie case of obviousness since proper motivation for one of ordinary skill to make the Examiner's proposed combination has not been established. Upon careful review of the applied prior art, we are in agreement with Appellant's stated position in the Briefs. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F. 2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

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As correctly pointed out by Appellant at pages 18 and 19 of the Brief, Anderson, while suggesting the appliance of a negative potential to a transistor source region to aid in the flow of electrons to a floating gate, never establishes the relationship of this negative potential to the power supply or ground voltages. Given this deficiency, we fail to see how the skilled artisan would find any suggestion or motivation in Anderson to modify Haddad in the manner proposed by the Examiner. In our view, even assuming, arguendo, that Haddad and Anderson could be combined, the resulting combination would not have suggested to one of ordinary skill the invention set forth in independent claims 43 and 51 which requires a particular relationship of voltages applied to the control gate and to the source or drain relative to the supply and ground voltages.

In summary, we are left to speculate why one of ordinary skill would have found it obvious to modify the applied prior art to make the combination suggested by the Examiner. The only reason we can discern is improper hindsight reconstruction of Appellant's claimed invention. In order for us to sustain the Examiner's rejection under 35 U.S.C. § 103,

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we would need to resort to speculation or unfounded assumptions or rationales to supply deficiencies in the factual basis of the rejection before us. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), reh'g denied, 390 U.S. 1000 (1968). Since we are of the view that the prior art applied by the Examiner does not support the rejection, we do not sustain the obviousness rejection of independent claims 43 and 51, nor of claims 6-9, 45, 46, and 52 through 57 dependent thereon.

In conclusion, we have not sustained any of the Examiner's rejections of the claims on appeal. Accordingly, the Examiner's decision to reject claims 6-9, 43, 45, 46, and 51-57 is reversed.

REVERSED

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KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	
Administrative Patent Judge)	APPEALS AND

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) INTERFERENCES
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STUART N. HECKER)
Administrative Patent Judge)

JFR:hh

VENABLE
POST OFFICE BOX 34385
WASHINGTON, DC 20043-9998