

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte MINORU ISHIDA and YUTAKA OKAMOTO

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Appeal No. 1997-3166  
Application No. 08/509,638

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HEARD: July 10, 2000

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Before THOMAS, KRASS, and BLANKENSHIP, Administrative Patent Judges. BLANKENSHIP,  
Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of Claims 15-28, all the claims remaining in the application.

We affirm-in-part and enter a new ground of rejection in accordance with 37 CFR

§ 1.196(b).

### BACKGROUND

The invention is directed to a unit memory cell of a static RAM. Claim 15 is reproduced below.

15. A unit memory cell of a static RAM comprising:

a flip-flop circuit including first and second inverters, said first inverter including a first driver transistor and a first load element and said second inverter including a second driver transistor and a second load element, first and second word transistors connected respectively to said first and second inverters, wherein a channel pattern for said first driver transistor of said first inverter and a channel pattern for said second driver transistor of said second inverter are symmetrical about a point, a channel pattern for said first word transistor and a channel pattern for said second word transistor are symmetrical about the point;

a channel pattern for said first load element of said first inverter and a channel pattern for said second load element of said second inverter are asymmetrical; and

a gate pattern for said first load element is different from a gate pattern for said second load element.

The examiner relies on the following references:

Oldham	4,396,996	Aug. 2, 1983
Nagayoshi et al. (Nagayoshi)	4,570,237	Feb. 11, 1986
Plus et al. (Plus)	4,833,644	May 23, 1989
Ikeda et al. (Ikeda)	4,841,481	Jun. 20, 1989
Kayama	5,241,204	Aug. 31, 1993 (filed Aug. 4, 1992)

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Claims 15, 16, 18, and 21-24 stand rejected under 35 U.S.C. § 102 as being anticipated by Oldham.

Claim 17 stands rejected under 35 U.S.C. § 103 as being unpatentable over Oldham and Kayama.

Claim 19 stands rejected under 35 U.S.C. § 103 as being unpatentable over Oldham and Plus.

Claim 20 stands rejected under 35 U.S.C. § 103 as being unpatentable over Oldham and Ikeda.

Claims 25-27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nagayoshi.

Claim 28 stands rejected under 35 U.S.C. § 103 as being unpatentable over Nagayoshi and Plus.

We refer to the Final Rejection (Paper No. 13) and the Examiner's Answer (Paper No. 21) for a statement of the examiner's position and to the Brief (Paper No. 19) and the Reply Brief (Paper No. 22) for appellants' position.

#### OPINION

##### Claims 15, 16, 18, and 21-24

The examiner has rejected Claims 15, 16, 18, and 21-24 as being anticipated by Oldham.

The examiner points to Figure 5 of Oldham, and text in columns 2 and 3, as the most pertinent portions

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of the disclosure. (See Answer, page 3.) Appellants argue that the reference does not disclose the physical layout of the device, but merely a schematic diagram of the circuitry, and that limitations in independent Claims 15 and 21 reciting physical placement of the semiconductor elements are thus not anticipated. (See Brief, pages 4-5.)

“Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention.” RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). We agree with appellants that the Oldham disclosure does not support a rejection for anticipation of the subject matter of Claims 15 and 21, respectively. Claim 15 recites, inter alia, that a channel pattern for the first driver transistor and a channel pattern for the second driver transistor are symmetrical about a point, and that a channel pattern for the first word transistor and a channel pattern for the second word transistor are symmetrical about the point. Oldham, however, merely shows transistors in schematic form, without the interrelated physical arrangement. Figure 5, that pointed out by the examiner, shows driver transistors (T1, T3) and load transistors (T2, T4), but the disclosure does not detail actual physical layout of all the elements.

Claim 15 also requires that “a channel pattern for [the] first load element...and a channel pattern for [the] second load element...are asymmetrical.” The examiner points to column 2, lines 40-46 of Oldham for material that is believed to read on the limitation. (See Answer, pages 3 and 6.) Column

1, line 67 through column 2, line 17, and column 2, lines 40 through 52 of the reference reveals that load transistors (T2, T4) are designed with different channel resistances. As a given example, if transistor T2 has a width to length ratio of 20:4, and transistor T4 has a width to length ratio of 15:4, then the channel resistance of T2 is lower than that of T4.

The reference thus discloses load transistors T2, T4 as having different width to length ratios, which would necessarily mean that the channel patterns for the first and second load elements are “asymmetrical.” Thus, while the reference meets the Claim 15 limitation concerning asymmetry of the channel patterns for the first and second load elements, the examiner has not pointed out any disclosure of the structures that are symmetrical about a point, as required by Claim 15. We therefore do not sustain the rejection of Claim 15. The rejection of Claims 16 and 18 is also not sustained, since each of the claims contain at least the limitations of Claim 15.

Claim 21 recites, inter alia, that “a channel of [the] first load transistor is longer than a channel of [the] second transistor.” However, as set forth above with respect to Claim 15, the reference’s explicit disclosure is that the width, rather than the length, differs between the channels of the load transistors. The lengths are disclosed as identical (i.e., four units). Whether the reference might suggest variations in length between the two transistor channels is not at issue. The rejection is for anticipation under 35 U.S.C. § 102. Because the reference does not disclose each and every element of Claim 21, we do not sustain the rejection made under Section 102. (We do, however, enter a new ground of

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rejection against the claim, infra, in accordance with 37 CFR § 1.196(b).) The rejection of Claims 22-24, dependent upon 21, is also not sustained.

#### Claims 17, 19, 20

The examiner has rejected Claim 17 over Oldham and Kayama, Claim 19 over Oldham and Plus, and Claim 20 over Oldham and Ikeda. Each rejection is under 35 U.S.C. § 103 for obviousness. (See Answer, pages 3-5.) However, the references of Kayama, Plus, and Ikeda as applied by the examiner fail to remedy the deficiencies with respect to Claim 15, identified supra. Since Claims 17, 19, and 20 each contain at least the limitations of base Claim 15, we conclude that the examiner has failed to set out a prima facie case for obviousness of the subject matter of the respective claims. We therefore do not sustain the rejections of Claims 17, 19, and 20.

#### Claims 25-28

In the Answer, new grounds of rejection were entered against Claims 25-27 as being anticipated by Nagayoshi. (See Answer, pages 5 and 6.) Claim 28 was rejected under 35 U.S.C. § 103 as unpatentable over Nagayoshi and Plus. (Id. at page 6.)

Appellants submitted a Reply Brief, but failed to respond to the Section 103 rejection. Accordingly, the appeal with respect to Claim 28 is dismissed. (See Answer, page 7.)

In regard to the Section 102 rejection over Nagayoshi, appellants argue that there are two voltage pattern lines running across the memory cell, and that there is no indication “that element 11(b) is connected to the second load element.” (Reply Brief, page 3.)

However, element 11b (Figure 4) of Nagayoshi is disclosed as being a ground line. As shown in the schematic diagram of Figure 2, each load transistor Tr3 and Tr4 is at least indirectly connected to ground. As detailed in column 2, lines 11 through 12 and column 3, lines 37 through 41, the electrical connections of the physical layout of Fig. 4 are disclosed in “Prior Art” Figure 2. Contrary to argument, element 11(b) of the reference is connected to at least the “second” load element, since it is connected to both load elements.

Regarding the arrangement shown in Figure 4 of Nagayoshi, while pattern line 11b clearly runs across the memory cell, we fail to see how voltage pattern line 11a might be thought to run “across” the memory cell. Pattern line 11a runs across, at most, structures comprising extensions of the memory cell. At oral hearing, counsel for appellants could not point to anything in the language of Claim 25 that sets forth anything different from the disclosure of Nagayoshi. We therefore sustain the rejection of Claims 25-27 over Nagayoshi.

New Ground of Rejection -- 37 CFR 1.196(b)

We enter the following new ground of rejection against the claims in accordance with

37 CFR 1.196(b): Claim 21 is rejected under 35 U.S.C. § 103(a) as unpatentable over Oldham.

Oldham discloses a memory cell comprising a flip-flop circuit with first and second inverters; see Fig. 1 and column 1, line 65 through column 2, line 20. The first inverter has a first driver transistor T1 and a first load transistor T2. The second inverter has a second driver transistor T3 and a second load transistor T4. The circuit includes a first word transistor T5 and a second word transistor T6. At least for the reason that first and second load transistors T2, T4 are distinct and separate physical structures, the “gate area” of the first is different from the “gate area” of the second. In addition, columns 3 through 5 of the written description detail forming the gate insulating layer of one load transistor differently from the other, succinctly set forth by Oldham in Claims 1 and 5 as the “means for selectively altering charge state.”

According to appellants, Claim 21 distinguishes over Oldham because “[t]here is neither teaching nor suggestion” of the Claim 21 limitation that ““a channel of said first load transistor is longer than a channel of said second load transistor.”” (Brief, page 5.) However, the reference details the following with respect to first and second load transistors T2, T4:

In order to insure that the memory cell (in connection with supply voltage  $U_{cc}$ ) flips into a predetermined position corresponding to a continuously stored digital information, the field effect transistors T2 and T4 are designed with different channel resistances. For this purpose, dimensions of their source-drain channels are embodied differently. If, for example, the transistor T2 has a channel width  $W$  which, with respect to its channel length  $L$ , is in a ratio of 20:4, while the quotient of channel width to channel length in the case of transistor T4, for example, is 15:4, then the channel resistance of T2, because of the larger channel width, is lower than that of T4.

Accordingly, the memory cell with connection of  $U_{cc}$  will constantly flip into the position in which node 3 lies approximately at the potential of the terminal lead 1 and node 4 lies approximately at the potential of terminal lead 2. The information stored in this manner can be used for test or checking purposes.

Oldham, column 2, lines 40 through 57.

Oldham thus teaches that the channel resistances of load transistors T2 and T4 should be different, and explicitly discloses that the “dimensions” of the channels should be embodied differently. Oldham gives an example of providing a different channel width to yield the desired difference in resistance. We find that the suggestion to vary dimensions of load transistors T2 and T4 would have led the artisan to investigate different combinations of the variations in the dimensions, including making one channel length longer than the other channel length. We conclude that, in view of the teachings of Oldham, the subject matter as a whole of appellants’ Claim 21 would have been prima facie obvious to the artisan at the time of invention.

#### CONCLUSION

The rejections of Claims 16-24 are reversed.

The rejections of Claims 25-27 are affirmed.

The appeal with respect to Claim 28 stands dismissed.

Claim 21 stands rejected under 35 U.S.C. § 103(a) over Oldham.

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This decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides that, "A new ground of rejection shall not be considered final for purposes of judicial review."

37 CFR § 1.196(b) also provides that appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (§ 1.197(c)) as to the rejected claim:

(1) Submit an appropriate amendment of the claim so rejected or a showing of facts relating to the claim so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART -- 37 CFR 1.196(b)

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Administrative Patent Judge	)	
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	)	BOARD OF PATENT
ERROL A. KRASS	)	APPEALS
Administrative Patent Judge	)	AND
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