THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 41

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HELGE NYLUND

Appeal No. 1997-3821
Application No. 08/570,256[1]

ON BRIEF

Before KRASS, MARTIN, and HECKER, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1-5,

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[1] Application for patent filed December 11, 1995.

8-13, 15, 16, 18-20, and 22-24, all of the pending claims.[2] We affirm-in-part.

A. The Invention

The invention relates to the architecture of a computer expansion board. The specification (at 2) describes the prior art as follows:

> The bits of data which define the information provided to the board are referred to as configuration bits and the act of providing the data bits to the board is referred to as configuring the board. Some boards are configured by manually operated switches which are connected to the board. These switches can be set prior to attaching the board to the host computer. When the board is powered up, the switches are read by the on board microprocessor or controller and the configuration information stored in the appropriate register for use as needed.
>
> In the past, the on board microprocessor or controller received the configuration bits on dedicated lines. Since the microprocessor or controller is typically implemented as an integrated circuit chip, each line requires an additional pin. The number of pins used solely for configuration bits will vary but in some LAN cards is thirty-two. Together with the various control,

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[2] The claims before us are the claims as amended in the amendment (paper no. 31) faxed to the PTO on August 28, 1996, which the examiner in a September 12, 1996, advisory action (paper no. 32) indicated would be entered upon the filing of an appeal. Although this amendment inadvertently has not yet been physically entered, it is being treated as such for purposes of this appeal.

> data and address lines, the total number of pins can exceed one hundred. In general, the cost of a chip increases with an increase in the number of pins. In addition, the cost of the board to which the chip is attached is also more expensive in order to accommodate the extra pins.

Referring to appellant's Figures 1A and 1B, the invention solves this problem by providing the expansion board 10, which has a connector 14 for insertion into an expansion slot (not shown) of host computer 12, with a memory 32 which stores configuration data for automatic transfer over the on-board internal parallel bus 30 to registers 18a and 18b of the on-board controller 16 when power is applied thereto. The memory 32 includes memory banks 34a and 34b, each of which contains a set of manual switches (36a, 36b) and a set of tri-state buffers (38a, 38b). The configuration data is read out of the tri-state buffers in memory banks 34a and 34b in response to signals provided on lines 40a and 40b, respectively, by the on-board controller.

B. The Claims

Of the appealed independent claims, i.e., claims 1, 10, 15, and 18, claim 15 is reproduced below as representative:

> 15. A method for configuring an expansion circuit board in an expansion slot having a connector, a

controller chip connected to the connector, an internal parallel data bus connected to said controller chip, transceiver means for controlling the transfer of configuration data bits from said expansion circuit board to a second parallel bus extending from a connector to a host computer and a memory connected to said internal parallel bus, comprising the steps of:

programming configuration data bits which define the address space occupied by said expansion circuit board with respect to a host computer into said memory, said configuration data bits enabling said host computer to communicate commands to and receive input from said expansion circuit board;

connecting said connector to said host computer, said controller chip being electrically coupled to said host computer when said connector is connected to the host computer, and said controller chip being electrically decoupled from the host computer when said connector is disconnected from the host computer;

determining when power is supplied to said controller chip and said other components of the expansion circuit board;

generating a control signal in response to said determining step;

providing said control signal to said memory; and

transferring said configuration data bits to said controller chip over said internal parallel bus independently of a command from said host computer, wherein, when said configuration data bits are transferred from said memory to said controller chip [sic].

C. The Reference and Rejections

The examiner relies on the following sole reference:

Morgan 4,980,850 Dec. 25, 1990

All of the appealed claims, i.e., claims 1-5, 8-13, 15, 16, 18-20, and 22-24, stand rejected under 35 U.S.C. § 103 for obviousness over Morgan.

Claims 15, 16, and 18-20 also stand rejected under the written description requirement of the first paragraph of § 112.

D. The § 112 Rejection of Claims 15, 16, and 18-20

The § 112 rejection was initially applied to all of the appealed claims in the final office action (paper No. 30) but was withdrawn with respect to all but claims 15, 16, and 18-20 as a result of the amendment (paper no. 31) filed August 28, 1996.

Independent claim 15 recites, inter alia, "determining when power is supplied to said controller chip and said other components of the expansion circuit board" and "generating a control signal in response to said determining step." The examiner contends that

the specification does not disclose the steps of

> determining when power is supplied to the controller as set forth in the claim (e.g. Claim 15 Lines 22-23). The claim language "determines" when the power is supplied. How can the system determine when the power is supplied when initially there is no power? The claim language is written as if some element is monitoring whether power is being supplied to the controller chip. What element does this monitoring? In order to perform this determining step it would seem that some element must be active to monitor the controller chip and "determine" when power is supplied. The specification is clear that initially no power is connected to the expansion board. When power is connected to the expansion board the controller executes a series of microinstructions (see P 5 Lines 26-27 of the Specification). The specification does not speak of monitoring the power or determining when the power is supplied, only that once it is supplied a series of microinstructions are executed. [Answer at 5.]

Appellant, after noting that Webster's New World Dictionary defines "determine" to mean "to fix" or "to ascertain" (Reply Brief at 2), argues that

> [t]he Specification provides at p. 5, lns. 26-30, "[w]hen power is provided to board 10, controller 16 executes a series of microinstructions." The plain language of the Specification thus requires the controller 16 "to fix" or "to ascertain" when it receives power so that it can execute a series of microinstructions. This is a well known operation in computer components. The previous examiner herself states that the computer of Morgan "determines" when power is supplied to the data processing system 10. (Answer at p. 4, lns. 16-19). [Reply Brief at 3.]

Appellant's reliance on the previous examiner's description of Morgan is misplaced, because unlike appellant's application Morgan discloses a separate power sensor element 28 for determining when power is initially applied to the data processing system 10:

> The present invention can also include means for sensing an initialization condition to cause the central processing unit to begin the initialization program. As shown in the preferred embodiment of the invention in FIG. 1, a power sensor 28 detects when electrical power is provided to data processing system 10 in order to initiate bootstrap operations. The output of circuit 28, after passing through synchronization circuitry not important to an understanding of the present invention, generates a reset (RST) signal for various components of data processing system 10 which take specific actions at times of initialization. [Col. 3, line 65 to col. 4, line 8.]

We find ourselves in agreement with the examiner on the support question. While appellant's specification states that "[w]hen power is provided to board 10, controller 16 executes a series of microinstructions" (p. 5, lines 26-27) and that "[o]nce the configuration data bits are written into registers 18a and 18b, controller 16 will continue its power up routine utilizing the configuration data bits to configure board 10" (p. 6, lines 8-11), it does not indicate that the

microcontroller or any other circuitry generates a signal which indicates that power has been applied and serves to instruct the microcontroller to commence the initialization program, as implied by the language in question. Accordingly, the § 112 rejection of claim 15 and its dependent claim 16 is affirmed.

However, the § 112 rejection is reversed with respect to independent claim 18 and its dependent claims 19 and 20, because claim 18 no longer includes the "determining when power is supplied" language that the examiner finds objectionable. Instead, the claim recites "said transferring steps are performed in response to the application of power to said expansion circuit board," which the examiner has not addressed.

E. The § 103 Rejection of Claims 1-5, 8-13, 15, 16, 18-20, and 22-24

Morgan discloses a data processing system 10 which provides
automatic configuration of memory boards 70, 72, 74, and 76, which, like appellant's expansion circuit boards, have connectors for insertion into expansion slots of a host

computer. However,

unlike appellant's expansion circuit boards, Morgan's expansion cards do not have microcontrollers. Instead, Morgan employs a central memory controller 30 located on the CPU board 15. The memory controller 30 includes a configuration status register 40[3] having configuration register circuits (200 in Fig. 2) for storing configuration data received over memory data bus 65 from the memory boards. Bank status register circuits 200

> each include a configuration register 202, a multiplexer 205, and a comparator 210. Each configuration register 202 contains configuration data about the memory bank corresponding to the bank status register circuit containing that configuration register. Bank status register circuits 200 cumulatively represent the configuration structure of the entire memory. [Col. 4, lines 61-68.]

In the preferred embodiment of memory board 70 shown in Fig. 5, signature register 160 holds configuration data for the corresponding memory banks on memory board 70 (col. 9, lines 42-45.) Preferably, the signature register is a set of pins which are connected to voltage sources each representing

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[3] Labeled in Figure 1 as a ?CONTROL STATUS REGISTER."

either a "1" or a "0" level (col. 9, lines 45-47.) Figure 8 is a flowchart showing the process by which configuration data is transferred via memory data bus 65 from signature register 160 of a memory card 70 to the configuration status registers 202 in configuration status register 40 of memory controller 30 (col. 12, line 23 to col. 13, line 2.) This process begins with CPU 20 setting the signature read request bit in the status configuration register 202 for one of the banks (Step 420 of Fig. 8) (col. 12, lines 25-29.)

We note that the claim language describing the location of the claimed "connector" could be more clear. Claim 1 recites, inter alia, "a host computer having an expansion slot," "a connector in the expansion slot being connectable to the host computer," and "an expansion circuit board in the expansion slot connected to said connector such that said connector is located between said expansion circuit board and said host computer" (our emphasis), which could be construed to mean that the connector is not part of the expansion circuit board. However, the claim further specifies that "said controller chip is electrically coupled to the host computer when said connector is connected to the host

computer, and said controller chip is electrically decoupled from the host computer when said connector is disconnected from the host computer," which makes it sufficiently clear from this language that the connector is carried by an edge of the expansion circuit board.

The examiner acknowledges that Morgan "does not specifically show a connector between the memory controller 30 and the CPU bus on CPU board 15 of Figure 1" (Answer at 3) and makes the following argument for adding such a connector:

> Since element 15 is described as a CPU board, it is reasonable to assume that CPU 20, boot ROM 22 and memory controller 30 would each be included in separate packages having pins to connect to the CPU bus. As the Applicant has stated, connectors are well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide some sort of connector between memory controller 30 and the CPU bus, and hence CPU 20. The Examiner also notes that [the] claims do not recite any special functionality pertaining to the connector. The specification does not even describe the connector in the abstract or summary and only briefly mentions it in one place, on page 4, line 4. [Answer at 3-4.]

The examiner's position is unpersuasive. The apparent reason the connector is not mentioned at all in the abstract or summary and is only briefly mentioned in the specification is that it was known to provide expansion circuit boards with

such connectors, which would be plugged into mating connectors in the expansion slots of computers, as implied by appellant's discussion of the prior art at pages 2 and 3 of the specification, quoted in part at page 2 of this opinion. Furthermore, while we agree with the examiner that it would have been obvious to provide Morgan's memory controller 30 as a package having connecting pins for engaging mating connectors on the CPU board 15, that modification would not satisfy the requirement of claim 1 and the other independent claims that the claimed controller chip, including its internal registers (Morgan's configuration registers 200 in configuration status register 40), be mounted on the expansion circuit board along with the claimed memory (Morgan's signature registers 160 - Fig. 5). On this point, the examiner further explains:

> Applicant also argues that there is no incentive to place the various elements on a single board as suggest[ed] by the Examiner (see P 16-17 of the Appeal Brief). It is a common practice in the art to move elements onto a common board to reduce cost and to increase reliability because there are less interconnections. In addition it has been held that making pieces separable/integral is a design choice. See Nerwin v. Erlichman, 168 USPQ 177 ([Bd. Pat. App.] 1969) and In re Larson, [340 F.2d 965,] 144 USPQ 347 (CCPA 1965). [Answer at 7.]

We do not agree that it would have been obvious to provide each of Morgan's memory boards 70, 72, 74, and 76 with a memory controller like Morgan's memory controller 30, including its configuration status registers 202 (Fig. 2). Because this modification would increase the total number of memory controller circuits, it would not reduce the cost, as urged by the examiner. Also, the examiner has not explained, and it is not apparent to us, why one skilled in the art would have concluded that such a modification of Morgan would result in fewer interconnections, as asserted by the examiner. This motivation instead appears to come from appellant's own disclosure, which of course is improper. See In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can only satisfy the burden to make out a prima facie case for obviousness by ?showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead the individual to combine the relevant teachings of the references”).

The examiner's reliance on Nerwin and Larson is also misplaced, as those cases concern mechanical inventions having interconnected parts.

For the foregoing reasons, we are reversing the § 103 rejection with respect to each of the appealed claims.

There is an additional reason for reversing the § 103 rejection of independent claims 1, 15, and 18, and their dependent claims 2-5, 8, 9, 16, 19, 20, 22, and 23. Each of these independent claims call for the transfer of configuration data from the claimed memory to the claimed internal register to occur "independently of a command from said host computer." We agree with appellant that this independence is not present in Morgan's system, wherein the process of transferring configuration data from configuration register 160 (Fig. 5) to configuration registers 202 (Fig. 2) is initiated by CPU 20, which sets a signature read request bit in the status configuration register 202 for one of the banks of memory (col. 12, lines 25-29.) The transfer of data is therefore dependent on (albeit indirectly) a command from the CPU.

F. Summary

The § 112, first paragraph, rejection is affirmed as to claims 15 and 16 and reversed as to claims 18-20. The § 103 rejection is reversed as to claims 1-5, 8-13, 15, 16,

18-20, and 22-24, i.e., all of the appealed claims.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ERROL A. KRASS Administrative Patent Judge	)
JOHN C. MARTIN Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
STUART HECKER Administrative Patent Judge	)

JCM:hh

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