

**THIS OPINION WAS NOT WRITTEN FOR PUBLICATION**

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 42

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte STEVEN S. LEE

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Appeal No. 1997-3979  
Application No. 08/586,365<sup>1</sup>

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ON BRIEF

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Before KRASS, MARTIN, and BARRY, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

**DECISION ON APPEAL**

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<sup>1</sup> Application for patent filed January 16, 1996, as a continuation of Serial No. 08/378,310, filed January 25, 1995, which is a continuation of Serial No. 08/082,694, filed June 28, 1993.

This is an appeal from the final rejection of claims 8-10 and 19, all of appellant's pending claims, under 35 U.S.C.

§§ 102 and 103. We reverse.

**A. The invention**

The invention relates to an BI-CMOS integrated circuit, i.e., an integrated circuit which includes bipolar junction transistors (BJTs), N-channel MOSFETs, and P-channel MOSFETs (Spec. at 1, lines 3-5).

Referring to Figure 7, a PG base layer which will be part of a BJT is formed by implanting boron into the N-well region through a layer of polysilicon and a layer of oxide (Spec. at 5, lines 24-26). The polysilicon scatters the boron atoms, reducing the channeling effect and thereby producing a PG layer that is thinner than would be the case if the implanting were not done in the absence of the polysilicon layer (Spec. at 5, line 26 to p. 7, line 5). The result is an improvement in the breakdown voltage of the base-emitter junction and a concentration of dopant that more closely approaches the step junction characteristic shown in Figure 12, thereby improving the speed and reliability of the transistor (Spec. at 7, lines

6-14). Figure 13, which incorrectly gives the depth dimension in microns rather than angstroms,<sup>2</sup> shows that when using an implantation energy of 30 KeV and oxide and polysilicon thicknesses of 130D and 500D, respectively, the peak concentration P3 of dopant occurs at a distance from the surface of between P1 (200 microns), and P2 (in the range of 700 to 1,000 microns) (Spec. at 7, lines 19-27).

**B. The claims**

Claims 8 and 19, the only independent claims, read as follows:

8. An intermediate structure from which a BICMOS integrated circuit can be constructed, comprising:

an oxide film coating a first N-well;

a polysilicon gate atop the oxide film; and

a second N-well, isolated from the first N-well, and having

a surface lacking substantial oxide and

a P-type layer adjacent the surface and having a peak doping concentration within the P-type layer at less than 700 angstroms from its upper surface.

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<sup>2</sup> The examiner apparently agrees with appellant's contention (Amendment filed June 21, 1996, paper No. 27, at 3) that "[t]he scale of Figure 13 should be angstroms, and not microns."

19. A p-type region in a semiconductor device having a peak doping concentration within the P-type region at less than 700 angstroms from its upper surface, wherein the P-type region is a base of a bipolar transistor, and wherein the semiconductor device further comprises MOS transistors.

**C. The references and rejections**

The examiner's rejections are based on the following prior art:

|                    |           |               |
|--------------------|-----------|---------------|
| Eklund             | 5,047,357 | Sep. 10, 1991 |
| Doki et al. (Doki) | 5,183,777 | Feb. 2, 1993  |

Claim 19 stands rejected under § 102(a) as anticipated by Doki.

Claims 8-10 stand rejected under § 103 for obviousness over Eklund in view of Doki.

**D. The § 102(a) rejection of claim 19 based on Doki**

Doki discloses a technique for forming a shallow junction having a thickness of 1,000Å or less and a high impurity concentration (col. 3, lines 18-22). This technique can be used to provide a semiconductor device having a shallow junction, such as a bipolar transistor or a MOS transistor, in which a channeling effect is prevented (col. 3, lines 23-26).

Figures 7A-7F show the technique being used to produce an MOS transistor (col. 6, lines 3-6), more particularly to produce the pG region 31 in Fig. 7D (col. 6, lines 28-35). Figures 8A-8E show the technique being used to produce a bipolar transistor (col. 6, lines 57-59), more particularly to produce the p-type base layer indicated as 42 in Fig. 8C (col. 7, lines 37-44). Figure 10 shows the impurity concentration S characteristic of a bipolar transistor base layer having a thickness of 40 nm, which is 400D (col. 7, lines 62-68). Figure 13B shows the impurity concentration characteristic for a base layer about 340D thick, formed in the presence of oxygen (col. 8, lines 37-43). Appellant argues that

[a]lthough Doki does teach how a shallow junction can be formed on either a FET device or a bipolar device, these descriptions are mutually exclusive of one another. There is simply no teaching or suggestion of forming such a shallow junction on a semiconductor device having both bipolar and MOS transistors (i.e. a BiCMOS device). [Brief at 5.]

That the examiner agrees with appellant that claim 19 calls for a BiCMOS device is apparent from the following argument:

While it is true that Doki does not explicitly recite forming both the bipolar and MOS transistors on the same substrate, note claim 19 only recites a shallow junction

device for the bipolar transistor. The MOS transistors are recited as merely present and are not claimed as shallow junction devices. Claim 19 is written broadly enough that the MOS transistor need not be part of the bipolar transistor as a so-called BICMOS structure but can be arbitrarily distant on the substrate or chip. The Abstract, line 1, of Doki recites "A method of forming a shallow junction..." and so is intended as a general method having general applicability. It will then be understood by one of ordinary skill in the art that other devices such as conventional MOS transistor[s] can be present since chips routinely have many thousands of devices integrated on the same substrate. [Answer at 3-4.]

We do not agree the term "a semiconductor device" in the preamble of claim 19 implies a BiCMOS device, i.e., a device in which a bipolar transistor and an MOS transistor are formed on the same substrate. The term "semiconductor device" is not defined in the application and therefore must be given its broadest reasonable interpretation consistent with appellant's disclosure as filed. See In re Morris, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997) (the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or

otherwise that may be afforded by the written description contained in the applicant's specification). In our view, the term "semiconductor device" is broad enough to read on a device containing a first integrated circuit chip which contains bipolar transistors and a second integrated circuit chip which contains MOS transistors. See TechEncyclopedia at <http://www.techweb.com/encyclopedia/defineterm?semiconductor+device> (June 30, 2000) (copy attached), which defines "semiconductor device" to mean "[a]n elementary component, such as a transistor, or a larger unit of electronic equipment comprised of chips".

Nevertheless, we are unable to sustain the § 102 rejection, because Doki fails to disclose a single semiconductor device, even in the broad "electronic equipment" sense, which contains both bipolar and MOS transistors. The examiner's argument that persons skilled in the art would have understood that bipolar and MOS transistors can be integrated on the same chip, even if broadened to mean that persons skilled in the art would have understood that bipolar and MOS chips can be used in the same piece of electronic equipment, is unconvincing because the argument goes to obviousness under

§ 103 rather than anticipation (e.g., by inherency) under § 102, which requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986).

The § 102 rejection of claim 19 over Doki is therefore reversed.

**E. The § 103 rejection of claims  
8-10 over Eklund in view of Doki**

Eklund discloses a method for forming an emitter junction for a bipolar transistor in a BiCMOS integrated circuit (col. 2, lines 33-48). Figures 3-10 show the construction steps of such a device, with Figure 3 showing an intrinsic base region 61 for constructing a bipolar transistor (col. 4, lines 3-10).

Figure 4 shows a mask 66 covering all but a small area over intrinsic base 61 to permit removal of the oxide layer 60 and polysilicon layer 64 over part of the intrinsic base region 61 in order to make room for an emitter contact (col. 5, lines 35-43). Referring to Figure 5, after the mask 6 is removed, a polysilicon layer 68 is deposited and then it and underlying

polysilicon layer 64 are implanted with two dopant species having different diffusion rates in silicon, such as phosphorous and arsenic (col. 5, line 43 to col. 6, line 4). Next, all of polysilicon layers 64 and 68 are removed except for the parts which are to function as gates 69g of the MOS transistors and as emitter contact 69e of the bipolar transistor (col. 6, lines 14-19). The implant conditions of the aforementioned arsenic and phosphorous implants may be adjusted independently from one another to optimize the emitter depth and conductivity desired for the structure (col. 6, lines 10-13). After completing the steps depicted by Figures 7-10, the structure is subjected to a high temperature anneal, which inter alia diffuses dopant from emitter electrode 69e into intrinsic base region 61 to form emitter region 89 therein, as shown in Fig. 10 (col. 7, lines 17-26). The specification explains that

the invention provides the advantage of a shallow emitter junction with a high impurity concentration in the emitter electrode 69e. In this embodiment, since emitter electrode 69e has both phosphorous and arsenic dopant species therewithin, the phosphorous implant dose may be selected to define the desired emitter junction depth, while the arsenic dose may be selected to

define the desired conductivity for emitter  
electrode 69e. [Col. 7, lines 43-51.]

Figure 11, which shows the dependency of junction depth on arsenic implant dosage when the phosphorus dosage is fixed at  $2E15$ , gives an emitter junction depth on the order of 140nm (col. 7, lines 51-61), which is 1,400D.<sup>3</sup> Figure 12, which shows the same relationship when the phosphorus dosage is fixed at  $5E15$ , gives an emitter junction depth on the order of 300nm (col. 7, lines 61-67), which is 3,000D.

The examiner reads the claimed elements on Eklund's Figure 10 as follows: the claimed "oxide film coating a first N-well" is read on N-well 20' and its overlying oxide layer (labeled 32 in Fig. 7); the claimed "polysilicon gate atop the oxide film" is read on the MOS transistor gate (69g in Fig. 9) and its underlying oxide layer (62 in Fig. 9); the claimed "second N-well, isolated from the first N-well" is read on N-well 20; and the claimed "surface lacking substantial oxide"

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<sup>3</sup>Because the depth scale indicates the combined thickness of the polysilicon layer and the emitter region, the examiner is incorrect to state that Figures 1, 2, 11 and 12 show an emitter depth on the order of 0.4 to 0.7 microns (Answer at 4-5).

is read on the upper surface of region 61, which at the stage of production shown in Figure 10 has had the emitter region 89 formed therein. We note that the foregoing limitations also can be read on the device in the production stage depicted in Figure 9, i.e., before the emitter region is formed in p-type region 61. The examiner concedes that claim 8's requirement that the p-type layer "hav[e] a peak doping concentration within the p-type layer at less than 700 angstroms from its upper surface" is not satisfied by Eklund. As evidence of motivation for forming Eklund's p-type layer with such a doping concentration, the examiner cites Eklund's disclosure that the shallower emitter region provided by his invention permits the use of a shallower base region, thereby allowing tighter control of a narrow base width (col. 1, lines 26-30) and yielding a higher performance transistor (col. 4, lines 18-29). In addition, the examiner notes Eklund's disclosure that the base and collector regions can be formed by conventional methods (col. 3, lines 59-64). Based on these suggestions and the fact that Doki's disclosed method produces a base region having a thickness as small as 340D (Doki's Fig. 13B), the examiner contends it would have been obvious to form

Eklund's p-type region 61 with a peak doping concentration within the p-type layer at less than 700 angstroms from its upper surface.

Appellant makes several arguments against obviousness. One is that the claimed device not Eklund's base region must be "relatively thick" because it must accommodate the thickness of the emitter region formed therein and that the artisan therefore "would not have been motivated to reduce the depth of the base region 61 to that of the claimed dimensions" (Brief at 8). We agree with this argument, which the examiner did not specifically address in the Answer. Although, as the examiner correctly notes, Doki discloses a base region whose peak doping concentration within the P-type layer is less than 700D from the upper surface (e.g., 340D as depicted in Fig. 13B), Eklund's p-type layer 61 must be thick enough to accommodate the emitter region 89, which is disclosed as having a thickness of 140nm, or 1,400D. Therefore, using Doki's technique to form Eklund's p-type region 61 would appear to result in a p-type region having a peak doping concentration located more than 1,400D from the surface of the p-type region, which is greater than the 700D permitted by

claim 8. The examiner has not explained, and it is not apparent to us, why the artisan would have understood Eklund to be teaching that his emitter region 89 can be made thin enough that his p-type region 61 can have a peak doping concentration which is less than 700D from the surface.

For the foregoing reasons, the § 103 rejection of claim 8 over Eklund in view of Doki therefore is reversed, as is the § 103 rejection of dependent claims 9 and 10 over those references.

We note in passing that appellant makes several other arguments that are not persuasive. The first is that whereas Eklund forms his base region 61 by implanting boron through the oxide layer 60 (col. 4, lines 12-17, citing application Serial No. 07/129,271), Doki's base-region formation technique requires more steps because part of the oxide layer 40 is removed to form an opening 39 (Fig. 8A) through which the base layer is created (col. 6, lines 60-68). According to appellant,

[a] person building BiCMOS devices would not have been motivated to add such additional masking steps to form a shallow junction, as they are motivated to reduce - or at least not increase - the number of masking steps in a

traditional process (see, for example, Applicant's specification, page 1, lines 14-18). [Brief at 7.]

This argument fails to take into account that the artisan may have been willing to increase the number of process steps in order to obtain a thinner base region and better transistor performance. See Winner Int'l Royalty Corp. v. Wang, 202 F.3d 1340, 1349 n.8, 53 USPQ2d 1580, 1587 n.8 (Fed. Cir. 2000) ("The fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another. Instead, the benefits, both lost and gained, should be weighed against one another.").

Appellant's other unpersuasive argument is that Doki's technique requires a second annealing at a temperature of 900 degrees C to form the source and drain regions of the MOS transistor (col. 6, lines 43-49) and that such thermal annealing would adversely impact any bipolar devices, as noted in appellant's specification at 5, second full paragraph. This argument is unconvincing because the rejection does not rely on Doki's disclosed technique for forming shallow source and drain regions in a MOS transistor. Instead, the

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rejection, which is motivated by Eklund's disclosure of making a bipolar transistor having a shallow emitter and base regions, relies on Doki only to the extent it discloses how to make a shallow p-type base region for a bipolar transistor.

**REVERSED**

|                             |   |                 |
|-----------------------------|---|-----------------|
| ERROL A. KRASS              | ) |                 |
| Administrative Patent Judge | ) |                 |
|                             | ) |                 |
|                             | ) |                 |
| JOHN C. MARTIN              | ) | BOARD OF PATENT |
| Administrative Patent Judge | ) | APPEALS AND     |
|                             | ) | INTERFERENCES   |
|                             | ) |                 |
| LANCE LEONARD BARRY         | ) |                 |
| Administrative Patent Judge | ) |                 |

JCM:hh

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