

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was **not** written for publication in a law journal and (2) is **not** binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEVEN P. HOUTCHENS

Appeal No. 1997-4217
Application No. 08/307,178

ON BRIEF

Before BARRETT, HECKER and LALL, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection¹

¹ An amendment after the final rejection (bearing the certified mailing date of October 15, 1996) is indicated to be filed as paper no. 16 and is indicated as approved for entry by paper no. 17. The amendment corrected only § 112, second paragraph, problems [brief, pages 1 and 2]. The Examiner's answer did not raise any § 112, second paragraph, problems, but only the section 103 rejection. It is clear that the amendment after the final rejection was in fact considered before the answer was written, even though the date of the entry of the amendment appears in the file record as after the dates of the briefs and the answers. So the claims as amended

(continued...)

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of claims 1 through 18, all the claims pending in this application. The disclosed invention relates to the simulation of a system having two continuous processes. The two processes are simulated independently and interact with each other by exchanging outputs. The outputs of each process are used as inputs to the other process. Each process has a different time step of simulation. A mechanical process has a long time step whereas an electrical process has a short time step. Regardless of the time steps and the rate of output signal changes, the two simulation processes need to be synchronized. In the claimed invention, one of the simulation processes is provided with the capability to back track to a previously simulated state when the simulation processes become out-of-synch. The invention saves the state of the first simulation process at the prescribed times. The

¹(...continued)
by said amendment are before us. There is a little confusion in that Appellant attached as Appendix II only the amended claims to the reply brief, leaving out the unamended claims. Also, Appellant attached all of the claims as Appendix I to the main brief, but they were the claims before the amendment. Thus, Appendices I and II each partially cover the claims on appeal.

invention tracks the state of each simulation process in order to determine when the simulation processes become out-of-synch and to back up and restore the simulated state to a previously synchronized state. The invention is further illustrated by the following claim.

1. A method for scheduling processes of a first simulator and a second simulator, the simulators having cross coupled first and second simulator inputs and outputs, the method being executed by at least one processor pursuant to program instructions of a control program stored in a memory coupled to said at least one processor, the first and second simulators stored as first and second simulation programs, respectively, in said memory and executed by said at least one processor, the method including the steps of:

(1) define an initial state, whereby said first and second simulator outputs are initialized and a verified simulation time (vt) and a first simulator current simulation time (ct_1) are set to an initial time value (t_0);

(2) select and store a target timepoint (tt) later than said first simulator current simulation time (ct_1);

(3) begin execution of said first simulator program using said second simulator outputs as initial simulator inputs;

(4) update said first simulator outputs by a first step time (at_1) not greater than said target timepoint (tt);

(5) define a second state, whereby said updated first simulator outputs do not equal said first simulator outputs;

(6) define a third state whereby said updated first simulator outputs equal said first simulator outputs;

(7) when said second state occurs store the simulation time at which said first simulator outputs changed as new target timepoint (tt);

(8) when said third state occurs continue updating said first simulator outputs stepwise at step (4) until said first simulator current simulation time (ct_1) equals said target timepoint (tt);

(9) post said updated first simulator outputs and target timepoint (tt) as new second simulator inputs to said second simulator and store a state of said first simulator;

(10) begin execution of said second simulator program using said second simulator inputs, with said verified simulation time (vt) as a current simulation time (ct_2) for said second simulator;

(11) update said second simulator outputs by a second step time (at_2) not greater than said target timepoint (tt);

(12) define a fourth state, whereby said updated second simulator outputs do not equal said second simulator outputs;

(13) when said fourth state occurs,

- a) store a simulation time at which the second simulator outputs changed as a new target timepoint (tt),
- b) post said changed second simulator outputs and said new target timepoint as new first simulator inputs to said first simulator,
- c) back up said first simulator to said verified simulation time (vt),
- d) generate new values for said first simulator outputs using said new first simulator inputs and said new target timepoint as an ending time for the simulation,

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e) store said new target timepoint as said verified simulation time and as said first simulator current simulation time (ct_1), and

f) continue until said verified simulation time equals a simulation completion time by proceeding to step 2;

(14) continue updating said second simulator outputs stepwise until said second simulator current simulation time (ct_2) equals said target timepoint (tt);

(15) store said new target timepoint as said verified simulation time and as said first simulator current simulation time (ct_1); and

(16) continue until said verified simulation time equals a simulation completion time by proceeding to step 2.

The references relied on by the Examiner are:

Catlin	4,814,983	Mar. 21, 1989
Judd et al. (Judd)	5,247,650	Sep. 21, 1993

Claims 1 to 18 stand rejected under 35 U.S.C. § 103 over Judd and Catlin.

Reference is made to Appellant's briefs and the Examiner's answers² for their respective positions.

² A reply brief was filed as paper no. 9 and the Examiner responded with a supplemental answer as paper no. 11.

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OPINION

We have considered the record before us, and we will reverse the rejection of claims 1 to 18.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In Re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293,

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227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. System., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In Re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Furthermore, the Federal Circuit states that “[the] mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.” In Re Fitch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), citing In Re Gordon, 773 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). “Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor.” Para-Ordnance Mfg. V. SGS Importers Int’l, 73 F.3d 1087, 37 USPQ 2d at 1239 (Fed. Cir. 1995), citing W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13 (Fed. Cir. 1983).

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ANALYSIS

We have reviewed Appellant's arguments [brief, pages 3 to 10 and reply brief, pages 1 to 9] and the Examiner's position [answer, pages 2 to 9 and supplemental answer, pages 1 to 4] and find that the suggested combination of Judd and Catlin does not meet the claimed method step to "back up said first simulator to said verified simulation time" (claim 1). The Examiner alleges at various places [answer, page 3 and supplemental answer, page 2] that "Judd disclosure would obviously imply the claimed back-up simulation process" [id. at 3] and that "Judd simulation system could be capable of backing up the other simulators in case of output state change . . ." [id. at 2]. However, we agree with Appellant that "[n]owhere does the undersigned attorney find anything in the cited portions of Judd to support the 'backup' phrase in the above recited sentence in the Examiner's Answer" [reply brief, page 6]. In fact, we also note, as does Appellant [brief, pages 4 to 5], that in Judd "[p]art of the centralized and local synchronization managers' task is to ensure that the simulated system continually moves forward in time and never

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backs up [in time]" (emphasis added). Note also that Judd clearly states that "[t]his ensures that each device 218 will never have to back up to a previous state and time." (Col. 14, lines 47 to 49). The other reference, Catlin, does not cure this noted deficiency. Catlin is not concerned about the synchronization of the simulation of multiple processes having different step time responses. Consequently, there is no need in Catlin to back up one process in time to catch up and get synchronized with another process. All the independent claims, 1, 2, 3, 4, 5, 11, 17 and 18 contain the same or similar limitation. Therefore, we do not sustain the obviousness rejection over Judd and Catlin of the independent claims 1, 2, 3, 4, 5, 11, 17 and 18 and, hence, their dependent claims 6 to 10, and 12 to 16.

In conclusion, the Examiner's decision rejecting claims 1 to 18 under 35 U.S.C. § 103 is reversed.

REVERSED

LEE E. BARRETT)
Administrative Patent Judge)
)

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STUART N. HECKER
Administrative Patent Judge

PARSHOTAM S. LALL
Administrative Patent Judge

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