

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRANCISCUS G.M. DE JONG
and MATHIAS N.M. MURIS

Appeal No. 1998-0069
Application 08/356,946¹

ON BRIEF

Before BARRETT, FLEMING, and HECKER, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

¹ Application for patent filed December 15, 1994, entitled (as amended in Paper No. 9) "Apparatus For Testing A Fixed Logic Value Interconnection Between Integrated Circuits."

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DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-17.

We reverse.

BACKGROUND

The disclosed invention is directed to a device and method for testing an interconnection between integrated circuits (ICs) having inputs with fixed logic values on a printed circuit board. Logic circuits utilize ICs which increasingly include Boundary Scan Test (BST) logic. These ICs enable testing of the interconnection function of the printed circuit board support in conformance with the BST method. IC inputs which are to receive a fixed logic value are usually provided with so-called pull-up or pull-down resistors, such as resistor 26 and resistors 22 in figure 1 to provide a logic "1" and logic "0," respectively. Special test points on the conductor and the resistor are required to test the interconnection to the IC. The interconnection between the input to a pull-up or pull-down resistor cannot be tested by the BST method because resistors do not comprise test logic. The invention provides fixed logic

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values from a sub-circuit 30 or 36 in the IC connected to BST cells 32 and 38 in figure 2 in an operational mode and test signals in a test mode, which allows testing of the interconnection by the BST method.

Claim 7 is reproduced below.

7. A method of testing an interconnection between an output of a means which, in an operational mode supplies a fixed logic value, and a signal input of an electronic circuit, the method comprising: (1) setting the means and the electronic circuit to a test mode through predetermined signals, (2) supplying test data to a first test connection of the means and transferring, via the output of the means, test data to the interconnection as an alternative to the fixed logic value, and (3) receiving result data in the electronic circuit via the signal input and transferring the result data to a second test connection of the electronic circuit for verification.

The Examiner relies on the following prior art:²

Jarwala et al. (Jarwala)	5,029,166	July
2, 1991		

² The Examiner also cites Sauerwald et al., U.S. Patent 4,879,717, Sauerwald et al., U.S. Patent 4,967,142, Tokuda et al., U.S. Patent 5,384,533, and Sullivan, U.S. Patent 5,487,074, in the list of prior art of record relied upon in the rejection of the claims under appeal (Examiner's Answer, page 3).

However, the references are not applied in any of the rejections. The listing of prior art in an Examiner's Answer should be limited to the references relied on in the rejections on appeal. See Manual of Patent Examining Procedure § 1208.

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Shiono et al. (Shiono) 5,390,191 February 14,
1995
(filed January 21,
1993)

Claims 1-17 stand rejected under 35 U.S.C. § 103 as
being unpatentable over Shiono and Jarwala.

We refer to the Final Rejection (Paper No. 10) (pages
referred to as "FR__") and the Examiner's Answer (Paper
No. 16) (pages referred to as "EA__") for a statement of the
Examiner's position and to the Appeal Brief (Paper No. 15)
(pages referred to as "Br__") and the Reply Brief (Paper
No. 17) (pages referred to as "RBr__") for a statement of
Appellants' arguments thereagainst.

OPINION

The issue is whether the combination of Shiono and
Jarwala teaches or suggests means that supplies a fixed
logic value to an output in an operational mode and which
can be set in a test mode to supply test data to the output
as an alternative to the fixed logic value signal.

The Examiner admits that Shiono does not disclose such
a means (EA5). The Examiner finds (EA5) that Shiono
discloses at column 6, lines 57-66, a holding mode in which
states of the integrated circuit do not change. While the

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reason for this finding is not clear, we speculate that the Examiner may be trying to analogize the fixed states in the holding mode to the claimed "fixed logic value signal." However, since the holding mode plainly occurs during the testing mode, Shiono does not disclose or suggest outputting a fixed logic value signal during an operational mode as claimed.

The Examiner finds that "Jarwala teaches (col. 4, lines 17-46) in his test apparatus comprising a memory which stores a map of the elements (boundary scan cells) and applies during operational mode individual bit of test vector to the test element" (FR3-4) and that Jarwala teaches "that (col. 4, lines 36-46) during operation, the control gate passes an individual bit to a separate one of the test elements" (FR4).

Appellants argue that the Examiner has misread Jarwala, because the phrase "[d]uring operation" (col. 4, line 36) is concerned with operation in a test mode, not the normal operational mode of the integrated circuits (Br7; RBr2). Appellants further argue that the output of the memory

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containing the map controls the multiplexer during testing, but does not appear at the output (RBr2).

We agree with Appellants that the portion of Jarwala relied on by the Examiner deals with the test mode, not with conventional operation. The Examiner does not refute this fact, but merely contends that the combined teachings of the references would have provided the motivation (EA9). Despite this lack of explanation, we consider Jarwala for what it would have suggested to one of ordinary skill in the art.

The Examiner's reliance on the BSC map is erroneous. The BSC map in the second memory 78 controls the multiplexer 76 to determine whether it outputs the non-conflicting test vectors from the first memory 70 or the sequence of vectors from the automatic test pattern generator (ATPG) 85. As noted by Appellants, the bits of the BSC map are not actually output. Apparently in response to Appellants' argument, the Examiner states that Jarwala includes a first memory whose output is supplied to a multiplexer which selectively outputs signals applied to one of its inputs and, thus, provides means to supply stored

values (EA8-9). Since the bits of the test vector in the memory 70 are output, we consider the Examiner's rejection as if it had been more accurately stated.

The portion of Jarwala at column 4 cited by the Examiner refers to the test data output (TDO) signal generator circuitry of figure 3 during a test mode. The TDO generator produces the test vector TD_0 , which is supplied to the circuits 12 in the boundary scan arrangement of figure 1 (col. 9, lines 59-62). The circuit of figure 3 supplies test vectors to avoid potential conflicts during testing. Jarwala is concerned with a controller structure for generating test vectors for the BSCs, not with a circuit that outputs either a fixed logic value in an operational mode or test data in a test mode.

We speculate that the Examiner is vaguely analogizing the multiplexer arrangement in figure 3 of Jarwala to the multiplexers in Appellants' figures 3 and 5. While it is true that Jarwala discloses a multiplexer that outputs either a bit of a test vector stored in the first memory 70 having a fixed value or a bit of a generated test vector from the ATPG 85, both bits are output in a test mode, not

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alternatively in an operational mode and a test mode. There is no suggestion in Jarwala that the functional signal from application logic 14 to one of the BSCs 16 in an IC 12 should have a fixed logic value during an operational mode. Furthermore, the circuit in figure 3 of Jarwala, discussed at column 4, corresponds to the TDO generator 60 in figure 2 which is part of the controller 22. The circuit supplies test data to the BSCs in the ICs 12 in figure 1 and is not part of the functional circuit connection in the ICs to the BSC; therefore, we fail to see how the Examiner proposes to modify Shiono in view of this teaching to arrive at the claimed subject matter.

The Examiner states (EA9): "Examiner takes official notice of the fact that due to recent advances in integrated circuit design and integration, Pull [sic] up and pull down resistors are being provided within integrated circuits thus providing fixed voltage levels and alleviating the need to add these on the circuit boards."

Appellants argue that this fact is not appropriate for official notice, but even if it is, it fails to meet the limitations of the present claims in which the point is not

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to eliminate pull-up and pull-down resistors, but to provide, during an operational mode, fixed logic level signals at the outputs of one device that are connected by way of circuit traces to inputs of other devices so that boundary scan testing of the electric connections between devices can be made (RBr4).

We agree with Appellants reasoning. Generation of an internal logic level value does not help to test the interconnection between devices having BSCs.

For the reasons stated above, we conclude that the Examiner has failed to establish a prima facie case of obviousness. The rejection of claims 1-17 is reversed.

REVERSED

LEE E. BARRETT)
Administrative Patent Judge)
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) BOARD OF
PATENT)
MICHAEL R. FLEMING) APPEALS

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Administrative Patent Judge)	AND
)	INTERFERENCES
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STUART N. HECKER)	
Administrative Patent Judge)	

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U.S. PHILIPS CORPORATION
Corporate Patent Counsel
580 White Plains Road
Tarrytown, NY 10591