

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KUO-TUNG CHANG

Appeal No. 1998-0343
Application 08/439,209

ON BRIEF

Before JERRY SMITH, GROSS, and BARRY, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 4-6, 8, 9, 16-25 and 28-33. Claims 1-3 have been allowed, claims 7 and 10-15 have been cancelled, and claims 26-27 have been indicated as containing allowable subject matter.

The disclosed invention pertains to an arrangement of components to form a nonvolatile memory structure.

Representative claim 4 is reproduced as follows:

4. A nonvolatile memory structure for storing a plurality of bits of data comprising:

a semiconductor substrate;

a first doped region and a second doped region, wherein the first and second doped regions lie within the substrate and are spaced apart from each other;

a channel region lying within the substrate and between the first and second doped regions;

a first gate dielectric layer overlying the substrate;

a first floating gate and a second floating gate overlying the substrate, wherein the first and second floating gates:

are spaced-apart from each other; and

each of the first and second floating gates does not extend across all of the channel region in any direction;

an intergate dielectric layer overlying the first and second floating gates;

a first conductive member and a second conductive member, wherein:

the first conductive member lies adjacent to the first floating gate and overlies a first portion of the channel region that is not covered by the first or second floating gates;

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the first conductive member is a gate for a first transistor and a control gate for a second transistor;

the second conductive member lies adjacent to the second floating gate and overlies a second portion of the channel region that is not covered by the first or second floating gates; and

the second conductive member is a control gate for a third transistor and a gate for a fourth transistor; and

the first and second conductive members are spaced apart from each other; and

a third conductive member overlying a third portion of the channel region that lies between the first and second conductive members, wherein the third conductive member is a select gate for the memory structure.

The examiner relies on the following reference:

Ma et al. (Ma)	5,278,439	Jan. 11, 1994 (filed Aug. 29, 1991)
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Claims 4-6, 8, 9, 16-25, and 28-33 stand rejected under 35 U.S.C. § 102(a) as being anticipated by the disclosure of Ma. We note that claims 20-22 depend from claim 1 which has been allowed by the examiner. Therefore, the rejection of these claims based upon the disclosure of Ma is clearly inappropriate. Rather than repeat the arguments of appellant or the examiner, we make reference to the brief and

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the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellant's arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the disclosure of Ma does fully meet the invention as set forth in claims 4-6, 8, 9, 16, 17, 19, 23-25, 28-31, and 33. We reach the opposite conclusion with respect to claims 18, 20-22, and 32. Accordingly, we affirm-in-part.

Anticipation is established only when a single prior art

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reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388

(Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

With respect to independent claims 4 and 23, the examiner indicates how Ma discloses a plurality of components of a nonvolatile memory structure [Answer, pages 4-5]. We note that the examiner's indication does not appear to correspond to any particular one of the claims on appeal nor address all the specific recitations of independent claims 4 or 23. In other words, the examiner's rejection simply points out that some of the claimed features are disclosed by Ma.

Appellant makes two primary arguments in support of his position that Ma does not fully disclose the claimed invention. First, appellant argues that Ma does not disclose the recitation that "each of the first and second floating gates does not extend across all of the channel region in any direction." Second, appellant argues that the examiner has improperly considered an array of memory cell structures in Ma rather than a single structure as claimed. The examiner disagrees with both arguments.

With respect to appellant's first argument, we agree with the examiner. We note that the channel region in question can be viewed as a three-dimensional volume bounded by the top surface of the substrate and having length, width and depth dimensions determined by the length, width and depth dimensions of the source and drain regions of the transistors. The depth dimension is clearly irrelevant here because the floating gates of the invention and of Ma are situated above the surface of the substrate. If one considers the space

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between the source and drain regions as the width dimension, it is clear that the floating gates 22B and 20B of Ma do not extend across all of channel region 22 in the width direction. The remaining length or vertical direction, as referred to by appellant, can best be seen in Figure 2B of Ma. We note that source and drain regions 22A and 20A in that figure are shown as rectangles which extend vertically beyond the floating gates in both directions. Since we view the channel region as defined by the length and width of the source and drain regions, we agree with the examiner that Ma's floating gates do not extend across all of the channel region in any direction.

With respect to appellant's second argument, we again agree with the examiner. We decline to interpret the claimed invention directed to a memory structure as limited to a memory cell structure. Although Ma's cell structure has only three transistors and appellant's cell structure has five transistors, we agree with the examiner that the claimed

memory structure can be read on the plurality of cells disclosed by Ma. The array of memory cell structures shown in Figure 3 of Ma has conductive members for forming control gates for four transistors consistent with the language of claim 4. Appellant's argument regarding Ma's use of "structure" in the singular or plural is irrelevant because Ma is describing a cell structure and a plurality of such cell structures form a memory structure.

Since we do not find either of appellant's arguments to be persuasive of error in the rejection of independent claims 4 and 23, we sustain the rejection of these independent claims as anticipated by the disclosure of Ma. Since appellant has not separately argued the patentability of dependent claims 5, 8, 9, 16, 17, 19, 24-31 and 33, these claims fall with independent claims 4 and 23.

Appellant argues dependent claim 6 separately [Brief, page 6]. Appellant's only argument is that Ma does not disclose different gate dielectric thicknesses. The examiner

points to Figure 4C of Ma and notes that dielectric layer 36C is shown as having a different thickness from dielectric layer 36A [Answer, page 7]. Although Ma does not specifically describe the thicknesses of layers 36C and 36A, we agree with the examiner that they are shown in the figure as being different. In the absence of any evidence that the different thicknesses shown in Ma were unintentional, we agree with the examiner that the invention of claim 6 is fully met by the disclosure of Ma.

Claims 18 and 32 are separately argued by appellant [Brief, page 6]. These claims recite that the memory structure has only five transistors. The examiner observes that the memory structure of Ma "has five transistors" [Answer, page 6], but the examiner never addresses the significance of the word "only" in these claims. It is clear that neither a single cell structure of Ma nor a plurality of cell structures in Ma has only five transistors. Therefore, the invention as set forth in claims 18 and 32 is not anticipated by Ma within the meaning of 35 U.S.C.

§ 102.

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Claims 20-22 are separately argued by appellant. As noted above, these claims depend from allowed claim 1. Therefore, the examiner's rejection of these claims is clearly inappropriate.

In summary, the examiner's rejection of the appealed claims is sustained with respect to claims 4-6, 8, 9, 16, 17, 19, 23-25, 28-31 and 33, but is not sustained with respect to claims 18, 20-22 and 32. Therefore, the decision of the examiner rejecting claims 4-6, 8, 9, 16-25 and 28-33 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JERRY SMITH)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ANITA PELLMAN GROSS))
Administrative Patent Judge)	APPEALS AND
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) INTERFERENCES
)
LANCE LEONARD BARRY)
Administrative Patent Judge)

JS:pgg
Harry A. Wolin
Motorola Inc.
Austin Intellectual Property Law Section
MD: TX32/PL02
7700 West Parmer Lane,
Austin, TX 78729