

The opinion in support of the decision being entered today was **not** written for publication in a law journal and is **not** binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KEITH S. ALBRIGHT

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Appeal No. 1998-1107  
Application No. 08/536,768

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ON BRIEF

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Before HAIRSTON, JERRY SMITH, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the rejection of claims 6-30. We reverse.

BACKGROUND

The invention at issue in this appeal relates to decimation filters. Decimation filters are used to decrease the sampling rate of data. In a conventional decimation filter, however, noise at frequencies above the base signal of

an input signal is aliased into the base signal. Once aliased therein, the noise cannot be removed by conventional filtering.

The invention uses a low pass filter stage to filter noise at frequencies above the base signal of an input signal. By filtering the noise before the decimation process, the noise does not get aliased into the base signal during decimation.

Claim 6, which is representative for our purposes, follows:

6. A method for digitally filtering a bit stream signal of one bit wide comprising the steps of:

a) delaying said bitstream signal in a plurality of serially connected delay stages;

b) summing together the true or complement of a selected group of said delay stages to form a summed signal, said group being greater than two; and,

c) integrating said summed signal in a plurality of integration stages to form a filtered output signal.

The references relied on in rejecting the claims follow:

Stehlik	5,517,529	May 14,
1996		filed Oct. 18, 1993
Scott et al. (Scott)	5,212,659	May 18,
1993.		

Claims 8, 9, 13, 26, and 27 stand rejected under 35 U.S.C. § 102(e) as anticipated by Stehlik. Claims 6, 11-12, 14-16, 18-25, and 28-30 stand rejected under 35 U.S.C. § 103 as obvious over Stehlik.<sup>1</sup> Claims 7, 10, and 17 stand rejected under 35 U.S.C. § 103 as obvious over Stehlik in view of Scott. Rather than repeat the arguments of the appellant or examiner in toto, we refer the reader to the brief and answer for the respective details thereof.

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<sup>1</sup> Although the examiner includes claims 29 and 30 in his statement of the rejection under 35 U.S.C. § 102(e), (Examiner's Answer at 4), the claims depend from claim 22, which is rejected under 35 U.S.C. § 103. Accordingly, claims 29 and 30 are more properly included with claim 22 in the latter rejection.

OPINION

In deciding this appeal, we considered the subject matter on appeal and the rejection advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellant and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 6-30. Accordingly, we reverse.

We begin by noting the following principles from Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997).

A prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim. See Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "[A]bsence from the reference of any claimed element negates anticipation." Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

We also note the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).... "A prima facie case of obviousness is

established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)). If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

With these principles in mind, we consider the appellant's argument and the examiner's reply.

The appellant argues, "Stehlik neither teaches nor suggests combining a select group of the true or complementary signals

from a series combination of delay stages to form a sum."  
(Appeal Br. at 20.) He adds, "[n]one of the delay circuits disclosed by Stehlik (shown as registers in the drawings, for example elements 172, 176, 178, 182, and 212) have the signals at a plurality of nodes summed together." (Id. at 21.) The examiner replies, "the adders included in the integrator cell circuits in Fig.'s 5B and 5C of Stehlik can also combine a select group of the true signals from a series combination of the delay stages to form a sum." (Examiner's Answer at 9.)

Claim 6 specifies in pertinent part the following limitations:

- a) delaying said bitstream signal in a plurality of serially connected delay stages;
  - b) summing together the true or complement of a selected group of said delay stages to form a summed signal, said group being greater than two
- ....

Similarly, claim 7 specifies in pertinent part the following limitations: "delaying said bit stream signal in a plurality of serially connected delay stages ...." Also similarly, claims

8-14 each specify in pertinent part the following limitations:

a series connection of delay stages having an input terminal for receiving an input signal and an output terminal, wherein a select group of the true and

complementary signals derived from the nodes of said series connection of delay stages are combined together in a combination circuit to provide a summed signal ....

Further similarly, claims 15-21 each specifies in pertinent part the following limitations:

a series connection of delay stages having an input terminal for receiving an input signal and an output terminal, wherein a select group of the true and complementary signals derived from the nodes of said series connection of delay stages are summed together to provide a summed signal ....

Similarly, claims 22-25, 29, and 30 each specifies in pertinent part the following limitations:

- a) a plurality of serially connected delay stages having an input terminal for receiving an input signal;
- b) a means for detecting the state of signals at selected nodes of said serially connected delay stages and for generating a sum signal which corresponds to the sum of one of the true or complement signals present at said selected nodes  
....

Also, claims 26-28 each specifies in pertinent part the following limitations:

the steps of integrating, summing, delaying, and decimating a data bit stream, wherein said summing step comprises summing one of the true or complement signals at a selected plurality of nodes of a delay circuit used to perform the delaying step ....

Accordingly, claims 6-30 require summing true or complement signals of selected nodes of a delay circuit. Claims 6-25, 29, and 30 further require that the delay circuit comprises a serial connection of delay stages.

The examiner fails to show a teaching or suggestion of the claimed limitations in the prior art. "The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not ... resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis." In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967).

Here, the examiner fails to map the exact and complete language of the claims to the teachings or suggestions of the references. Instead he broadly observes, "Stehlik uses Hogenaur filters comprising a plurality of delay stages, adders, inverters, and integrators (see Fig.'s 5A-C and col. 7, lines

21-67)." (Examiner's Answer at 9.) The reference teaches a decimation filter stage comprising myriad components.

Specifically, Stehlik includes the following description.

The first decimation filter stage **124, 126** is illustrated in FIG. 5A. Each filter **124, 126** includes a cascaded integrator filter section **170** having a number of integrator cells **171**; a first register **172** following the cascaded integrator filter section **170**; a cascaded comb filter section **173** having a number of comb cells **174**; and a second register **176** following the cascaded comb filter section **173**.

Col. 7, ll. 39-45. The examiner fails to explain, however, which of these components he believes constitutes a delay circuit comprising a serial connection of delay stages.

The examiner's reply that "the adders included in the integrator cell circuits in Fig.'s 5B and 5C of Stehlik can also combine a select group of the true signal from a series combination of the delay stages to form a sum," (Examiner's Answer at 9), is also inexact. Stehlik teaches an integrator cell comprising plural components and connections.

Specifically, Stehlik includes the following description.

An example of an integrator cell **171** is shown in FIG. 5B and includes a register **178** and an adder

**180.** The operation of these integrator cells **171** is well known in the art and is described in the Hogenaur article cited above. In the integrator register **172**, the digital signal input from the heterodyning circuit **122**, and filtered by the cascaded integrator filter section **170**, is subsampled by, as in the example described herein, a factor of 8, thereby effecting an 8:1 rate change.

Col. 7, ll. 46-56. The examiner fails to explain, however, which of these components and connections he believes sums true or complement signals of selected nodes of a delay circuit. The examiner also fails to allege, let alone show, that Scott cures these deficiencies.

In view of these failures, we are not persuaded that the references disclose or would have suggested the claimed limitations of summing true or complement signals of selected nodes of a delay circuit or a delay circuit comprising a serial connection of delay stages. Therefore, we reverse the rejection of claims 8, 9, 13, 26, and 27 as anticipated by Stehlik; the rejection of claims 6, 11-12, 14-16, 18-25, and 28-30 as obvious over Stehlik; and the rejection of claims 7, 10, and 17 as obvious over Stehlik in view of Scott.



Administrative Patent Judge )           AND  
  )   INTERFERENCES  
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LANCE LEONARD BARRY                 )  
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