

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KYOJI MARUMOTO

Appeal No. 1998-1114
Application 08/353,254¹

ON BRIEF

Before HAIRSTON, BARRETT, and RUGGIERO, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed December 2, 1994, entitled "Semiconductor Memory Apparatus Having A Protecting Circuit," which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Application 5-303609, filed December 3, 1993.

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This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 13-16. Claims 1-12 have been canceled.

We reverse.

BACKGROUND

The disclosed invention is directed to a semiconductor memory incorporating a protecting circuit to prevent data stored in a memory portion from being read out and illegally copied. The protecting circuit is shown in figure 3. Memory portion 1 is blocked from being read out to a terminal 11 by a three-state buffer 4a. Key release data is input to input register 25 via terminal 11 when the three-state buffer is in a high-impedance state. When the key release data matches stored key data in key memory 24, the flip-flop 22 is set which cancels the high-impedance state of the buffer 4a and allows data to be read.

Claim 13 is reproduced below.

13. A semiconductor memory apparatus, comprising:
a memory portion storing a program;
a terminal for external connection;

a three-state buffer, one end of said three-state buffer is connected to said memory portion so that said three-state buffer can receive program data from said memory portion, and another end of said three-state buffer is connected to said terminal for external connection, said three-state buffer being capable of taking a high-impedance state in addition to two-value states of high-level and low-level;

- a key memory for storing key data;

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an input register, connected to said terminal for external connection, for storing a key release signal received via said terminal when said three-state buffer is in the high-impedance state;

an RS flip-flop connected to said three-state buffer, for turning said three-state buffer into the high-impedance state to disconnect said memory portion from said terminal under a reset state and for canceling the high-impedance state under a set state;

a power-on reset circuit for resetting said RS flip-flop when a power is turned on; and

a comparator for comparing an output from said key memory and an output from said input register to set said RS flip-flop when the two outputs coincide.

The Examiner relies on the following prior art:

Wong et al. (Wong)	4,933,577	June 12, 1990
Yaezawa	5,377,343	December 27, 1994

The contents of Yaezawa and Wong are adequately described by Appellant (Brief, pp. 8-9).

Claims 13-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yaezawa and Wong.

We refer to the Final Rejection (Paper No. 8) and the Examiner's Answer (Paper No. 15) (referred to as "EA__") for a statement of the Examiner's position, and to the Brief (Paper No. 14) (pages referred to as "Br__") for a statement of Appellant's arguments thereagainst.

OPINION

Appellant argues (Br8) that the combination of Yaezawa and Wong fails to teach or suggest the limitations of claim 13 that (1) a comparator sets the RS flip-flop when the output from the key memory and the output from the input register coincide, and (2) the RS flip-flop turns a three-state buffer into a high-impedance state or cancels the high-impedance state. The Examiner breaks limitation (2) into three parts: (2) Yaezawa does not disclose the use of a tri-state buffer; (3) Yaezawa does not disclose controlling the tri-state buffer with the output of the R-S flip-flop; and (4) Wong does not disclose controlling a tri-state buffer with a flip-flop (EA7).

We also find that the combination of Yaezawa and Wong does not teach or suggest the input register connected to the same terminal as a three-state buffer; however, since this limitation is not argued, it will not be further addressed. See 37 CFR § 1.192(c)(8)(iv) (1996) ("For each rejection under 35 U.S.C. 103, the argument shall specify the errors in the rejection and, if appropriate, the specific limitations in the rejected claims which are not described in the prior art

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relied on in the rejection, and shall explain how such limitations render the claimed subject matter unobvious over the prior art."). Cf. In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art.").

The Examiner states (EA7-8):

[S]ome of the above identified differences are at least partially taught by elements of the prior art. To wit:

With respect to difference (1), Yaezawa teaches the use of a comparator circuit (Fig. 1, element 6) connected to a key memory (Fig. 1, element 2) and an input register (Fig. 1, element 4), while Wong teaches the use of an R-S flip-flop (Fig. 4, element 52).

Additionally, with respect to difference (2), Wong discloses the use of a tri-state buffer (Wong at abstract and Fig. 4, element 62).

. . .

Finally, with respect to differences (3) and (4), it is the Examiner's position that one of ordinary skill in the art would have found these differences to have been obvious at the time the invention was made. A proper analysis of these differences, therefore, begins with an inquiry into who one of ordinary skill in the art would be[.]

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The Examiner errs by trying to dispose of difference (1) by pointing to individual elements in Yaezawa and Wong without providing any motivation or explanation why it would have been obvious to combine the elements in the manner claimed, i.e., the comparator sets the RS flip-flop when the output from the key memory and the output from the input register coincide.

The Examiner finds, based on a discussion of the enormous economic investment and the costs associated with errors in design in satellite broadcasting and gaming technology (EA8-10), that the level of knowledge and the level of ordinary skill in the art was very high (EA10): "[I]t would be indisputable that one of ordinary skill in the art would be someone of extraordinary skill. For example, one of ordinary skill would be someone with (1) a BSEE degree, and (2) an advanced degree (e.g.: MSEE or Ph.D.), as well as substantial (i.e., 10+ years) experience in electronics design of critical components."

The Examiner has attempted to make a finding as to the level of art, which is relied on in the obviousness conclusion. Although we do not disagree with the Examiner's ultimate finding, we see some problems. First, mere

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discussion without citation of a reference presents an evidentiary problem because there is no way for anyone to verify the truth of the statements. "Even if obviousness of the variation is predicated on the level of skill in the art, prior art evidence is needed to show what that level of skill was." In re Kaplan, 789 F.2d 1574, 1580, 229 USPQ 678, 683 (Fed. Cir. 1986). Thus, although we believe the Examiner's discussion leading to the finding is correct, if we were to adopt the finding there would be no way for a court reviewing our decision to verify whether we were correct. Second, mere numbers of years of education and/or experience are unhelpful to resolving the obviousness question because it says nothing about what was concretely presumed to be known as a result of that education and experience. It is much more useful to find that one of ordinary skill in the art knew something specific, such as "one of ordinary skill in the art of memory protection had a working knowledge of computer and memory architecture." Third, the simpler approach to show the level of ordinary skill, consistent with Kaplan, is to find the references to be representative of the level of ordinary skill in the art. See In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978)

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("the PTO usually must evaluate both the scope and content of the prior art and the level of ordinary skill solely on the cold words of the literature"); In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (the Board did not err in adopting the approach that the level of skill in the art was best determined by the references of record).

The Examiner finds that "[c]omparators, R-S flip-flops, and tri-state buffers are common components" (EA11) and that "even one with a low degree of skill in electronics design would know how to use a comparator to compare an input with a key, then send the results of the comparison to a R-S flip-flop to store the state of the last performed comparison, and then to use the state stored within the flip-flop to operate a device with multiple modes, such as a tri-state buffer" (EA11).

The issue is whether it would have been obvious to one of ordinary skill in the art to arrange the elements as claimed without the benefit of Appellant's disclosure, not whether one skilled in the art would have known how to do what is claimed once told how to do it. Thus, the Examiner's finding is not helpful to the obviousness analysis because it fails to state

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why one of ordinary skill would have arranged the elements as claimed without using Appellant's disclosure as a guide.

The Examiner concludes that "[i]n view of the high level of skill which must be attributed to one of ordinary skill in this art, . . . such a person at the time the invention was made would have found it obvious to have combined Yaezawa and Wong to have arrived at the invention as claimed in claims 13-16 because such a combination would reduce costs" (EA11), where "the reduction of cost is an important factor in the field of endeavor" (EA11).

We fail to see how the extremely general motivation of reducing cost would have suggested the specific modifications necessary to result in the claimed subject matter. While there are some circumstances where a modification may be suggested by cost considerations (e.g., to combine functions to reduce the number of parts or the assembly time), we find no direct relationship between cost and the modifications required to produce the claimed subject matter in this case and the Examiner has pointed to none. The Examiner does not explain how he proposes to combine the teachings of Yaezawa and Wong, or provide technical reasons why one of ordinary

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skill in the art would have been motivated to make the changes. Moreover, since Yaezawa shows an R-S flip-flop, but does not show a tri-state buffer, and since Wong shows an R-S flip-flop and a tri-state buffer, but not a tri-state buffer controlled by the output of the R-S flip-flop, there must be some teaching in the knowledge of those skilled in the art that would suggest combining Yaezawa and Wong so as to have the R-S flip-flop control the tri-state buffer. However, we find no specific teaching or discussion of this limitation.

As to the Examiner's conclusion that the invention would have been obvious because the level of ordinary skill in the art is very high, "this observation alone cannot supply the required suggestion to combine these references."

In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998). As stated in Rouffet, id.:

While the skill level is a component of the inquiry for a suggestion to combine, a lofty level of skill alone does not suffice to supply a motivation to combine. Otherwise a high level of skill in an art field would almost always preclude patentable inventions. As this court has often noted, invention itself is the process of combining prior art in a nonobvious manner. . . . Therefore, even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. . . . In other words, the Board must explain the reasons one of ordinary skill in the art would have been

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motivated to select the references and to combine them to render the claimed invention obvious.

One cannot simply provide a stack of references showing bits and pieces and rely on the high level of skill in the art to make unspecified modifications to produce the claimed subject matter.

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In conclusion, the Examiner has failed to establish a prima facie case of obviousness. The rejection of claims 13-16 is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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