

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KAZUO NAKAIZUMI

Appeal No. 98-1643
Application 08/544,582¹

ON BRIEF

Before THOMAS, KRASS, and DIXON, Administrative Patent Judges.
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of
claims 1 through 17. The examiner has withdrawn the final
rejection of claims 1 through 17 under 35 U.S.C. 112, first

¹ Application for patent filed October 18, 1995.

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and second paragraphs. Since, as to the remaining rejection, claims 3 through 17 are now indicated as being directed to allowable subject matter, the appeal before us involves only claims 1 and 2.

The invention is directed to a tester for integrated circuits wherein testing functions are performed by both a semiconductor chip and a testing set for inputting signals to an integrated circuit under test. The semiconductor chip is in direct contact with the integrated circuit under test.

Representative independent claim 1 is reproduced as follows:

1. A tester for integrated circuits, comprising:

(a) a testing set for supplying inputs to an integrated circuit under test for operation thereof and for measuring outputs of said integrated circuit under test; and

(b) a semiconductor chip or wafer arranged to be in direct contact with said integrated circuit under test, said semiconductor chip or wafer having at least one testing function for testing said integrated circuit under test.

The examiner relies on the following reference:

Leedy	5,020,219	Jun. 4,
1991		

Claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as anticipated by Leedy.

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Reference is made to the brief and final rejection and answer for the respective positions of appellant and the examiner.

OPINION

We affirm.

The examiner appears to rely on two different embodiments of Leedy as support for the rejection. The examiner relies on the embodiment of Fig. 4a of the reference for the teaching of a testing set and, apparently, on the embodiment of Fig. 14 of the reference for the teaching of a semiconductor chip or wafer (134) in direct contact with the integrated circuit under test (133) and having at least one testing function.

We do not agree with appellant's argument that it is improper for the examiner to rely on elements of two separate embodiments of a reference. A rejection under 35 U.S.C. § 102(b) requires a disclosure of the claimed subject matter in a single reference. Leedy is a single reference and we find no impropriety in relying on different teachings within

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that single reference in making an anticipation rejection under 35 U.S.C.

§ 102(b).

With regard to whether the examiner's reliance is indicated by Leedy itself, we are of the view that it is. The embodiment of Fig. 4a shows a tester signal processor for providing inputs to an integrated circuit under test and for measuring outputs of the integrated circuit. This would appear to be not much different than what appellant shows as the prior art in instant Figures 1 and 2 wherein a main frame 51 has a CPU, 61, therein for supplying the inputs and measuring outputs to and from the integrated circuit under test.

The Fig. 14 embodiment of Leedy then indicates that the tester logic circuits are actually placed on, or in contact with, the integrated circuit to be tested. However, even in the Fig. 14 embodiment, there clearly are inputs to, and measurements from, the integrated circuit under test. Either the inputs are provided by tester circuit 134 itself, in which case the tester circuit must receive those inputs from some other source, or input signals are provided to the circuit

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under test directly from that outside source. Since there must be some source providing the input signals and measuring the output signals, then that would be suggestive of using the outside source, i.e., the tester signal processor, shown in the Fig. 4a embodiment.

Thus, if there is an outside source inputting the signals to, and receiving the output signal from, the circuit under test, then there is the suggestion of the two separate elements, i.e., a "testing set" and "a semiconductor chip or wafer," required by instant claims 1 and 2.

Even if there is no outside source shown in Fig. 14 of Leedy and the signals are input from, and outputted to, the tester/logic circuit 134, itself, the claim language is still met because the "testing set" of the claims, as broadly recited, is not required to have any testing function. The claims only require that the "testing set" supply inputs to the circuit under test and measure outputs from the circuit under test. Clearly, something provides the input signals to, and measures outputs from, the circuit under test. Either such is supplied by an outside source, as suggested in Fig. 4a of Leedy, in which case this is exactly what is claimed and

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intended, or, in the alternative, the tester/logic circuit 134 provides the input signals to, and measures outputs from, the circuit under test, in which case the instant claims are still met since one might argue that the claims are broad enough to permit one element to be both the "testing set" and the "semiconductor chip or wafer...in direct contact with said integrated circuit under test."

Appellant's arguments are clearly narrower than the instant claim language would require. That is, in accordance with the instant claim language, a single element may perform the functions of *both* the claimed testing set *and* the semiconductor chip or wafer in direct contact with the circuit under test. Further, the instant claim language does not require the testing set to actually have any testing function (it merely supplies inputs to, and measures outputs from, the circuit under test) and certainly no testing function separate and apart from the testing function of the semiconductor chip or wafer.

Thus, we find that Leedy's disclosure does anticipate instant claims 1 and 2 under 35 U.S.C. § 102(b). The examiner's decision is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

	James D. Thomas)	
	Administrative Patent Judge)	
)	
)	
	Errol A. Krass)	BOARD OF
PATENT	Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
	Joseph L. Dixon)	
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tdc

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