

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAROSLAV HYNECEK and MATTHEW J. FRITZ

Appeal No. 1998-1698
Application No. 08/411,033

ON BRIEF

Before THOMAS, BARRETT, and DIXON, **Administrative Patent Judges**.
DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1-6 and 9-14. Claim 7 is objected to as dependent on a rejected parent claim and claim 8 has been canceled.

We REVERSE.

BACKGROUND

The appellants' invention relates to a circuit and technique for smear subtraction in CCD image sensors. The invention increases the charge capacity of the image sensing area during charge transfer to memory which allows the entire charge including the portion due to smear to remain with the image charge so that it may be subtracted without eliminating a portion of the image charge. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. An image sensing device comprising:

an image sensing area having a lateral overflow antiblooming drain structure; and

a frame memory area coupled to the image sensing area for storing charge from the image sensing area, wherein during charge integration, the antiblooming drain is biased at a first level, and during charge transfer to memory, the antiblooming drain is biased at a second level such that the image sensing area will have a higher charge capacity than during the charge integration.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Hieda et al. (Hieda)	4,782,394	Nov. 1, 1988
Stevens (Stevens '183)	4,949,183	Aug. 14, 1990
Higashitsutsumi	5,089,894	Feb. 18, 1992
Stevens et al. (Stevens '774)	5,130,774	Jul. 14, 1992

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Claims 1, 5, 6, and 9 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hieda in view of Stevens '774. Claims 2, 3, 10, and 11 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hieda and Stevens '774 in view of Stevens '183. Claims 4 and 12-14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hieda, Stevens '774 and Stevens '183 in view of Higashitsutsumi.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 12, mailed Nov. 13, 1997) for the examiner's reasoning in support of the rejections, and to the appellants' brief (Paper No. 11, filed Aug. 8, 1997) for the appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

For a rejection under 35 U.S.C. § 103, the examiner is required to provide a reason from some teaching, suggestion or implication in the prior art as a whole, or knowledge generally available to one of ordinary skill in the art, why one having ordinary skill in the

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pertinent art would have been led to modify the prior art to arrive at the claimed invention. **Uniroyal, Inc. v. Rudkin-Wiley**, 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), **cert. denied**, 488 U.S. 825 (1988). These showings by the examiner are an essential part of complying with the burden of presenting a *prima facie* case of obviousness. **Note In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Furthermore, "[o]bviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." **Para-Ordnance Mfg., Inc. v. SGS Importers Int'l Inc.**, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), citing **W.L. Gore & Assocs., Inc. v. Garlock, Inc.**, 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983).

While appellants' arguments are quite brief and generally address the references and the language of claims 1 and 9, appellants argue that neither Hieda nor Stevens '774 teaches biasing the lateral overflow antiblooming drain at two different voltages to increase the capacity of the image sensing area during charge transfer to memory. (See brief at page 6.) We agree with appellants.

The examiner relies upon Hieda (answer at page 4) for a teaching that two voltages are used in the accumulation and elimination of unwanted charge. Furthermore, we note that the examiner relies upon multiple embodiments of Hieda in the rejection to reconstruct appellants' claimed invention. The examiner maintains that Hieda discloses that the

storage capacity of the imaging part 2 is increased during the integration period T_2 , but the language of claim 1 requires that the increase of capacity occurs due to “biasing” of the lateral overflow antiblooming drain structure at a second level. While Hieda appears to contain parts of the claimed invention, the examiner has not shown that the teachings from the two embodiments can be integrated into a single system. (See answer at page 4.) Moreover, the examiner has not shown why the skilled artisan would have been motivated to vary the bias voltage to increase the capacity of the imaging area during charge transfer to memory. Hieda discloses that there is a difference between the two embodiments at column 10, line 9 through column 11, line 9. Hieda states:

[t]he first embodiment, as described above, is arranged in such a manner that the anti-blooming means in the image pickup means is intermittently operated during the integration period for accumulating unwanted charges which are to be eliminated and are not used, and is continuously operated during the substantial integration period for accumulating wanted charges.

The second preferred embodiment of the present invention will now be described in connection with FIGS. 10 through 13. This second embodiment is arranged in such a manner as to more efficiently eliminate the unwanted charges during the unwanted charge integration period T_2 .

The second embodiment is characterized in that the accumulation quantity of the unwanted charges is limited in advance by reducing the maximum possible accumulation quantity of the unwanted charges in the imaging part 2 of the CCD 1 (FIG. 1) during the unwanted charge integration period as compared with that during the substantial integration period.

FIG. 10 shows a timing chart of driving pulses generated in the second embodiment for limiting the maximum accumulation quantity of the charges

in the imaging part 2 of the CCD 1 during the unused charge integration period.

In FIG.10, vertical transfer pulses NI and NS substantially corresponding to the number of vertical picture elements or rows in the imaging part 2 are generated twice, that is, shortly before the beginning of the vertical blanking period and shortly after the vertical blanking period, thereby obtaining the shortened substantial integration period T_1 . Also, the anti-blooming gate pulses NABG are applied continuously during the period T_1 and are applied intermittently during the period T_2 . In addition, in the second embodiment, during the accumulation of the unwanted charges, the level of the pulses NI is set not to the middle level 1M but instead to the low level 1L in order to increase the efficiency of the charge elimination through the regions ABG. This decreases the quantity of charges which remain in the picture elements in the imaging part 2.

The reason for this level setting will be explained with reference to FIGS. 11(a) and 11(b). FIGS. 11(a) and 11(b) show potential distributions in the imaging part 2 when the level of the pulse NI is at the level IM and IL respectively. In FIG. 11(a), the sum of the charges Q1 accumulated in each region CW and the charges Q2 accumulated in each region VW after the elimination of excess charge through the regions ABG becomes the maximum charge quantity. On the other hand, in FIG. 11(b) the sum of the charges Q3 accumulated in each region VW after the elimination of excess charges through the regions ABG becomes the maximum charge quantity. Apparently, the quantity of charges which remain at the end of the unwanted charge integration period T_2 is decreased more in FIG. 11(b) than in FIG. 11(a), thus reducing the quantity of charges which are to be eliminated by vertical transfer, and thereby decreasing the overflow of charge which takes place during the vertical transfer period of the charges at the beginning of the substantial integration.

Also, as is understood from the comparison between FIGS. 11(a) and 11(b), since the storage capacity of the imaging part 2 during the period T_2 is increased, it is possible to reduce the likelihood that the excess charges would overflow from the imaging part 2 to the storage part 3 and destroy the signal to be read out from the storage part 3.

Here, Hieda reduces the capacity for accumulation of charge during the unwanted charge integration period as compared with that during the substantial integration period rather than increasing the capacity. While these capacities have a difference between the wanted and unwanted charge integration periods, the examiner has not addressed the difference and why skilled artisans would have been motivated to have the difference as recited in the language of claim 1.

We note that the examiner has not stated that during the charge transfer to memory that the drain structure been biased, nor has the examiner addressed the limitation of biasing as opposed to the application of a series of pulses. According to The American Heritage® Dictionary of the English Language¹, “bias” is defined as the fixed voltage applied to an electrode and “biasing” is defined as applying a small voltage to (a grid). Here, the examiner has not addressed the biasing of the lateral overflow antiblooming drain structure as recited in the language of claim 1.

The examiner relies upon Hieda at col. 8, lines 29-32, for the knowledge that it is possible to vary the antiblooming ability, and therefore, skilled artisans would have desired to vary the ability to increase or decrease the capacity of the imaging area. To place this

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citation by the examiner in proper context, we include the entire paragraph in which the citation is found. Hieda states at column 8, lines 10-47 that:

the charges accumulated during the period T_2 are not used and are eliminated, while the charges accumulated during the following period T_1 are read out and used. Thus, in this case the period T_1 is a substantial integration period. When a large quantity of charge is accumulated during the period T_2 , even if charge transfer is carried out at some intermediate point, the unwanted charges may not be completely eliminated, so that a certain quantity of harmful charge may remain in the imaging part 2. For this reason, in this embodiment, the anti-blooming gate pulses NABG are applied to the electrode 2ABG intermittently, i.e., during each horizontal blanking period HBLK, (which is the low level period of a horizontal blanking pulse HBLK shown in FIG. 7) so as to reduce the quantity of charge to be accumulated during the period T_2 . Furthermore, during the substantial integration period T_1 , it is preferable to successively apply the anti-blooming gate pulses NABG to the electrode 2ABG to prevent blooming. It is possible to vary the anti-blooming ability or power by changing the frequency and/or amplitude of the anti-blooming gate pulses NABG to be applied to the electrode 2ABG. Either method may be adopted, depending on circumstances. Here, if the anti-blooming gate pulses NABG are successively applied to the electrode 2ABG during the long period T_2 , noise would be introduced at the output amplifier 5 and would harm the displayed image on the screen. This would also be disadvantageous in terms of power consumption because of the successive high frequency pulses. To solve this problem, in this embodiment, the anti-blooming gate pulses NABG are applied intermittently, i.e., only during each horizontal blanking period in the period T_2 . Applying the anti-blooming gate pulses NABG only during each horizontal blanking period is advantageous, since the noise due to the pulses NABG is concentrated in the horizontal blanking period and therefore the displayed image is not harmed.

Here, Hieda is concerned with the elimination of unwanted changes which may be harmful, therefore, the anti-blooming gate pulses NABG are applied to the electrode 2ABG

intermittently, i.e., during each horizontal blanking period HBLK, (which is the low level period of a horizontal blanking pulse HBLK shown in FIG. 7) so as to reduce the quantity of charge to be accumulated during the period T_2 .

The examiner relies upon Stevens '774 to teach the use of a lateral overflow drain antiblooming structure and that it would have been obvious to one of ordinary skill in the art at the time of the invention to include this into the system of Hieda. (See answer at pages 4-5.) Appellants argue that Stevens '774 does not disclose or suggest the change of the charge capacity of the image sensing area because the lateral overflow drain and the image sensing area are controlled by the same gate. (See brief at pages 6-7.) We agree with appellants that Stevens '774 is silent with respect to any control of the capacity of the imaging area.

From our review of Steven '774, we find that Stevens '774 merely teaches the structure of a lateral overflow drain and reduction of cross talk. Since Hieda does not clearly disclose the control of charge capacity by varying a bias voltage to increase the capacity during the charge transfer to memory and Stevens '774 does not remedy the deficiency in Hieda, we cannot sustain the rejection of claim 1 and its dependent claims 2-8. Independent claim 9 contains similar limitations which the combination of Hieda and Stevens '774 do not teach or suggest. Therefore, we cannot sustain the rejection

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of claim 9 and its dependent claims 10-14. The examiner has not relied upon the teachings of Stevens '183 or Higashitsutsumi to remedy the above noted deficiencies in the combination of Hieda and Stevens '774. Similarly, we find that they do not remedy the above noted deficiencies.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-6 and 9-14 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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